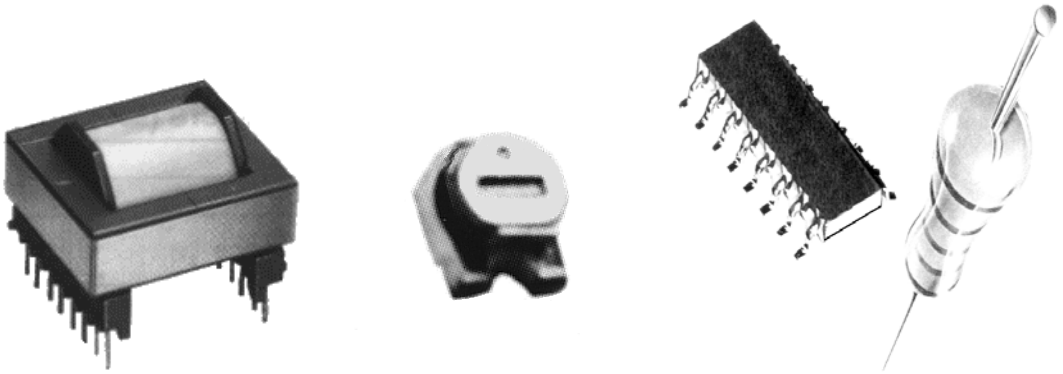
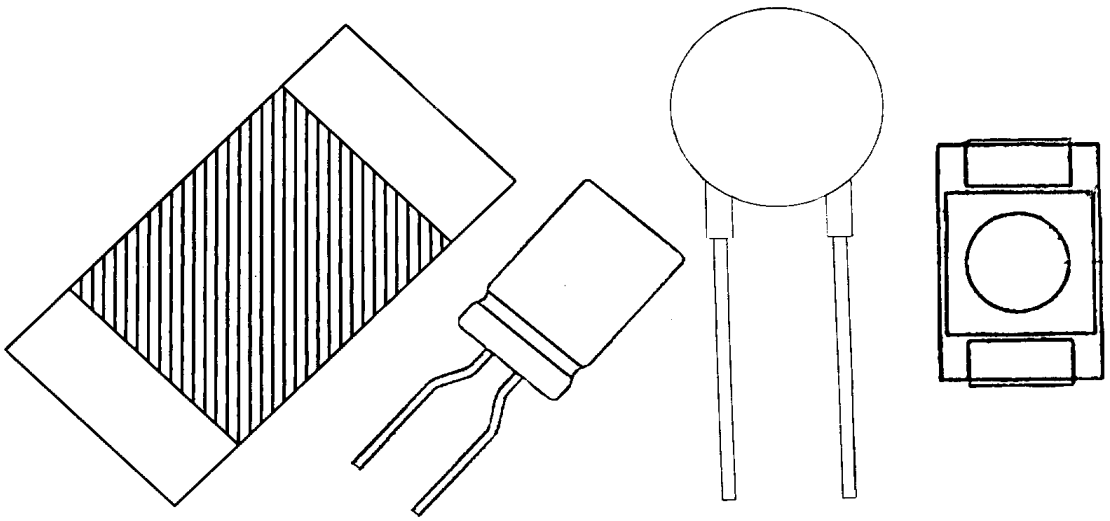
AEC-Q200-REV C
June 17, 2005



STRESS TEST QUALIFICATION FOR PASSIVE COMPONENTS



Automotive Electronics Council
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STRESS TEST QUALIFICATION FOR PASSIVE ELECTRICAL DEVICES

1.0 SCOPE

1.1 Description

This specification defines the minimum stress test driven qualification requirements and references test conditions for qualification of passive electrical devices. This document does not relieve the supplier of their responsibility to meet their own company's internal qualification program. In this document, "user" is defined as all companies that adhere to this document. The user is responsible to confirm and validate all qualification and assessment data that substantiates conformance to this document.

1.1.1 Definition of Stress-Test Qualification

Stress-Test “Qualification” is defined as successful completion of test requirements outlined in this document and any applicable supplements and compliance to any applicable user packaging specification. The minimum temperature range required for each passive electrical component type is listed below (maximum capability) as well as example applications typical of each grade (application specific):

GRADE	TEMPERATURE RANGE		PASSIVE COMPONENT TYPE Maximum capability	TYPICAL/EXAMPLE APPLICATION
	MINIMUM	MAXIMUM		
0	-50°C	+150°C	Flat chip ceramic resistors, X8R ceramic capacitors	All automotive
1	-40°C	+125°C	Capacitor Networks, Resistors, Inductors, Transformers, Thermistors, Resonators, Crystals and Varistors, all other ceramic and tantalum capacitors	Most underhood
2	-40°C	+105°C	Aluminum Electrolytic capacitors	Passenger compartment hot spots
3	-40°C	+85°C	Film capacitors, Ferrites, R/R-C Networks and Trimmer capacitors	Most passenger compartment
4	0°C	+70°C		Non-automotive

Qualification of the noted device type to it's minimum temperature grade allows the supplier to claim the part as "AEC qualified" to that grade and all lesser grades. Qualification to temperatures less than the minimum specified above would allow the supplier to claim the part as "AEC qualified" at the lower grade only.

1.1.2 Approval for Use in an Application

“Approval” is defined as user approval for use of part in the application. The user’s method of approval is beyond the scope of this document.

1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

1.2.1 Military/EIA

1. EIA-469	Destructive Physical Analysis (DPA)
2. MIL-STD-202	Test Methods for Electronic and Electrical Parts
3. EIA-198	Ceramic Dielectric Capacitors Classes I,II,III,IV
4. EIA-535	Tantalum Capacitors
5. J-STD-002	Solderability Spec
6. JESD22	JEDEC Standard
7. MIL-PRF-27	Test Methods for Inductors/Transformers

1.2.2 Industrial

1. UL-STD-94	Test for Flammability of Plastic Materials
2. ISO-7637-1	Road Vehicle Electrical Disturbance

1.2.3 AEC

1. AEC-Q200-001	Flame Retardance Test
2. AEC-Q200-002	ESD (Human Body Model)
3. AEC-Q200-003	Beam Load (Break Strength) Test
4. AEC-Q200-004	Polymeric Resettable Fuse Test
5. AEC-Q200-005	Board Flex Test
6. AEC-Q200-006	Terminal Strength Test
7. AEC-Q200-007	Voltage Surge Test

2.0 GENERAL REQUIREMENTS

2.1 Objective

The objective of this document is to ensure the device to be qualified meet the qualification requirements detailed in Tables 2 - 14.

2.2 Precedence of Requirements

In the event of conflict in the requirements of this specification and those of any other documents, the following order of precedence applies:

1. The purchase order
2. The user’s individual device specification
3. This document
4. The reference documents in Section 1.2 of this document
5. The supplier's data sheet

For the device to be considered a qualified part, the purchase order and/or individual device specification cannot waive or detract from the requirements of this document.

2.3 The Use of Generic Data to Satisfy Qualification and Requalification Requirements

The use of generic data for qualification will be based on a matrix of specific requirements associated with each characteristic of the device and manufacturing process as shown in Tables 2-14 and Appendix 1.

Tables 2A-14A define a set of qualification tests that must be considered for any changes proposed for the component. Tables 2A-14A matrix is the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and user should use as a baseline for discussion of tests that are required for the qualification in question. All items in Tables 2-14 are tests that are required during component qualification and must be considered during the development of a component qualification plan. It is the supplier's responsibility to present rationale for why any of these tests need not be performed.

Appendix 1 defines the criteria by which components are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable to the qualification of the device in question.

With proper attention to these qualification family guidelines, information applicable to other devices in the family can be accumulated. This information can be used to demonstrate generic reliability of a device family and minimize the need for device-specific qualification test programs. This can be achieved through qualification of a range of devices representing the “four corners” of the qualification family (e.g. highest/lowest voltage, high/mid/low value). Sources of generic data shall come from certified test labs, and can include internal supplier's qualifications, user-specific qualifications and supplier's in-process monitors. The generic data to be submitted must meet or exceed the test conditions specified in Tables 2-14. End-point test temperature must address worst-case temperature extremes and designed product life for the applications. The user(s) will be the final authority on the acceptance of generic data in lieu of specific device test data (to include temperature ranges of the devices.)

2.3.1 Wearout Reliability Tests (End of Life Testing)

Testing for the failure mechanisms specific to each component technology should be available to the user whenever a new technology or material relevant to the appropriate wearout failure mechanism is to be qualified. The data, test method, calculations, and internal criteria need not be demonstrated or performed on the qualification of every new device, but should be available to the user upon request.
Note: This information may be subject to a confidentiality agreement, since it contains proprietary information of the supplier.

2.4 Test Samples

2.4.1 Lot Requirements

Lot requirements are designated in Table 1, herein.

2.4.2 Production Requirements

All qualification parts shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at projected production volumes.

2.4.3 Reusability of Test Samples

Devices used for nondestructive qualification tests may be used to populate other qualification tests. Devices that have been used for destructive qualification tests may not be used any further except for engineering analysis.

2.4.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 1. If the supplier elects to submit generic data for qualification, the specific test conditions and results must be reported. Existing applicable generic data shall first be used to satisfy these requirements and those of Section 2.3 for each test required in Table 1. Such generic data shall not be more than 2 years old. Part specific qualification testing shall be performed if the generic data does not satisfy these requirements.

2.4.5 Pre and Post Stress Test Requirements

All endpoint test temperatures (room, hot and cold) are specified in the "Additional Requirements" column Tables 2-13 for each test. The specific value of temperature must address the temperature extremes and designed product life for the application for at least one lot of data (generic or part specific) submitted per test. For example, if the supplier designs a device intended solely for use in a Grade 3 environment (e.g. -40°C to +85°C), his endpoint test temperature extremes need only address those application limits. Qualification to applications in higher-grade environments (e.g. -40°C to +125°C for Grade 1) will require testing of at least one lot using these additional endpoint test temperature extremes. All endpoint test conditions must include all user specifications for any given family.

2.5 Definition of Test Failure After Stressing

Test failures are defined as those devices not meeting the individual device specification, post-test criteria specific to the test or the supplier's data sheet in order of significance as defined in Section 2.2. Any device that shows external physical damage attributable to the environmental test is also considered a failed device. If the cause of failure is agreed (by the manufacturer and the user) to be due to mishandling or ESD, the failure shall be discounted, but reported as part of the data submission.

2.6 Criteria for Passing Qualification

Passing all appropriate qualification tests specified in Tables 1 and 2-14, either by performing the test (acceptance of zero failures using the specified minimum sample size) on the specific part or demonstrating acceptable family generic data (using the family definition guidelines defined in Appendix 1 and the total required lot and sample sizes), qualifies the device per this document.

Passing the acceptance criteria of all the tests in Table 1 and the conditions in Tables 2-14 qualify the device per this document. When the number of failures for any given test in Table 1 exceeds the acceptance criteria using the procedure herein, the device shall not be qualified until the root cause of the failure(s) is (are) determined and the corrective and preventive actions are implemented and confirmed to be effective in an 8D or other acceptable user format. New samples or data may be requested to verify the corrective and prevented action.

Any unique reliability test or conditions requested by the user and not specified in this document shall be agreed upon between the supplier and user requesting the test, and will not preclude a device from passing stress-test qualification as defined by this document.

2.7 Alternative Testing Requirements

The users, through supporting data presented by the supplier demonstrating equivalency, must approve any deviation from the test requirements, listed in Table 1 and the test conditions listed in Tables 2-14. These deviations will be clearly reported when the results of the qualification are submitted to the user for approval.

3.0 QUALIFICATION AND REQUALIFICATION

3.1 Qualification of a New Device

Requirements for qualification of a new device are listed in Table 1, with the corresponding test conditions listed in Tables 2-14. For each qualification, the supplier must present data for ALL of these tests, whether it is stress test results on the device to be qualified or acceptable generic family data. A review is to be made of other parts in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the user.

For each part qualification, the supplier must present a Certificate of Design, Construction and Qualification data see Appendix 2.

3.2 Qualification of a Lead (Pb) – Free Device

Added requirements needed to address the special quality and reliability issues that arise when lead (Pb) free processing is utilized is specified in Section 4. Materials used in lead-free processing include the termination plating and the board attach (solder). These new materials usually require higher board attach temperatures to yield acceptable solder joint quality and reliability. These higher temperatures will likely adversely affect the moisture sensitivity level of plastic packaged devices. As a result, new, more robust mold compounds may be required. If an encapsulation material change is required to provide adequate robustness for Pb-free processing of the device, the supplier should refer to the process change qualification requirements in this specification. Preconditioning should be run at the applicable reflow temperatures described in Section 4 wherever it is required before environmental stress tests.

3.3 Requalification of a Device

Requalification of a device shall be required when the supplier makes a change to the product and/or process that impact the form, fit, function, quality and reliability of the device.

3.3.1 Process Change Notification

The supplier shall submit a projection to the users of all forecasted process changes. This projection of implemented changes shall be submitted at least 6 months in advance. Information required for submission to the user will include the following as a minimum:

1. Benefit to the user (value, time and quality).
2. For each user part numbers involved in the change, the following information is required:
   a) Supplier part number
   b) An estimated date of the last production lot of unchanged parts.
   c) An estimated final order date and final ship date of unchanged parts.
   d) The first projected shipment date and date code of changed parts.

A detailed description of the change in terms of the materials, processes, visual/electrical/mechanical characteristics, rating, circuit design, internal element layout and size as applicable.

4. Technical data and rationale to support the proposed changes.
5. An electrical characterization comparison (between the new and original product) of all significant electrical parameters over temperature extremes that the change could affect. Changes in median and dispersion performances shall be noted even though conformance to specification limits is still guaranteed.
6. The supplier shall submit an updated Certificate of Design, Construction and Qualification along with information required by this section (section 3.2.1) plus any changes impacting Appendix 2 information as originally submitted.
7. The results of completed supplier Requalification tests of the changed device(s).

Items 1, 2, 3, & 4 are background information needed up front to evaluate the impact of the change on supply and reliability and to come to agreement on a qualification plan acceptable to the supplier and user. Items 5, 6 and 7 must be submitted prior to any final approval to implement any change on the user's product. **No change shall be implemented without prior approval of the users.**

3.3.2 Changes Requiring Requalification

As a minimum, any change to the product, as defined in Appendix 1, requires performing the applicable tests listed in Tables 1 and 2-14. Table 2A-14A will be used as a guide for determining which tests need to be performed or whether equivalent generic data can be submitted for that test. These tables include requirements for comparative testing of parts produced before the change to parts produced after. At a minimum, electrical characterization test #19 should be performed on a comparative basis. An agreement between the supplier and the user(s) with justification for performing or not performing any recommended test shall occur before the implementation of a Requalification plan.

3.3.3 Criteria for Passing Requalification

It is the responsibility of each user to review the data, change notices, and supporting documentation to either qualify or not qualify the change based on the results of the tests performed. All criteria requirements described in 2.6 apply.

3.3.4 User Approval

A change may not affect a part's qualification status, but may affect its performance in an application. Individual user authorization of a process change will be required for that user's particular application(s), and this method of authorization is outside the scope of this document.

4.0 QUALIFICATION TESTS

4.1 General Tests

Test details are given in Tables 1-14. Not all tests apply to all devices. For example, certain tests apply only to hermetically packaged devices, others apply only to SMD large can devices, and so on. The applicable tests for the particular device type are indicated in the "Note" column of Table 1 and the "Additional Requirements" in Tables 2-14. The "Additional Requirements" column of Tables 2-14 also serves to highlight test requirements that supersede those described in the referenced test.

4.2 Device Specific Tests

The following tests must be performed on the specific device to be qualified for all devices. Generic data is not allowed for these tests. Device specific data, if it exists, is acceptable.

1. Electrostatic Discharge (ESD) - All product.

2. Electrical Characterization - The supplier must demonstrate that the part is capable of meeting parametric limits detailed in the individual user device specification. This data must be taken from at least three lots of the required sample size over the specified temperature range.

3. Additional Environmental Testing may be required because of the user's experience with the supplier.

4.3 Lead (Pb) – Free Specific Tests

4.3.1 Solderability

The qualification requirements outlined in Table 4.1 are to act as a supplement to EIA/JESD22-B102 Solderability Test Method. **The solderability (test #18) and resistance to solder heat (test #15) tests are still required to be performed on Pb-free components for backward compatibility with Pb processes.** A single lead-free solder solution has not been industry standardized as has eutectic tin-lead solder. For different formulations of solder, the chemistry, reflow temperatures and joint reliability may vary widely. Thus, until one can be standardized, the supplier must use the user's recommended solder and flux for performing solderability testing for that user. Steam age preconditioning is performed before the solderability test to simulate the oxidation of the termination plating that can develop over a long storage time. This oxidation can minimize the solder coverage via pinholes, voids, porosity, nonwetting and dewetting and produce poor solder strength or poor reliability.

Table 4.1 – Solderability Requirements for Forward/Backward Compatibility

Qualification Requirements	Pb-free component Forward compatibility	SnPb terminated component Backward compatibility
Solderability Test Reference	JESD22 Method B102	JESD22 Method B102
Aging Preconditioning	8 hours steam aging	8 hours steam aging
Solder Composition	Sn-Ag(3.5+/-0.5%)-Cu(0.5+/-0.1%)	Eutectic Sn (63 wt%) – Pb (37 wt%)
Flux	no-clean RMA	no-clean RMA
Solder Dip Temperature/Time	260 (+0/-5) ^{O}C 10 seconds max.	220 (+5/-0) ^{O}C 10 seconds max.
Solder Bath Contaminant	Manufacturer's recommended limits	Manufacturer's recommended limits

4.3.2 Preconditioning and Environmental Stress Test Requirements

The table in this section below serves as the recommended environmental tests that the supplier should consider when qualifying a new or changed Pb-free component. The supplier can propose, with technical justification, a subset of the recommended tests for a given component type.

A typical manufacturing requirement is the ability of the component to withstand up to 3 reflows at Pb-free conditions (e.g., top-side, bottom-side, rework). The table in this section below reflects the current mechanical limitations of specific types of passive components in meeting this requirement.

Preconditioning is used to simulate the thermal stress devices must endure during attachment to circuit boards in electronic system manufacturing. These stresses become more severe and, thus, more important to simulate when higher Pb-free temperatures are used. These stresses can then influence the functional life of the device, which is why preconditioning is required before environmental life stress tests.

4.3.3 Passive SMD Device Preconditioning

Refer to Table 4.2 to determine the maximum number of reflows before the appropriate reliability stress test for a given type of passive component. The difference in the number of reflows represents the differences in capability among the various types of passive devices. The peak reflow temperature for Pb-free forward compatibility, measured as the reflow oven ambient, is 260(+0/-5)^{O}C when attaching surface mount passive devices onto test boards. If the supplier feels their component cannot endure a 260^{O}C reflow and demonstrate acceptable life, perform a lower reflow precondition temperature, informing the user immediately of this deviation.

Table 4.2 – Preconditioning Reflow Requirements Before Reliability Stress Testing

ISSUE	PASSIVE DEVICES							
Qualification Requirements	AEC-Q200							
SMD Moisture Preconditioning	JEDEC JESD22-A113 A/ Number of reflow passes required onto test boards is shown per test and type of component. Number is dependent on technology limitations.							
Required Reliability Stress Tests after Preconditioning / Type of Component	HTE	TC	MR	BH	OL	TS	Term Str	Bd Flex
Ceramic/Tantalum Capacitor	3	3	3	3	3	3	3	3
Electrolytic/Film Capacitor C/	2	2	2	2	2	2	2	2
Resistor		3			3	3	3	3
Inductor	2	2	2	2	2	2	2	2
PTC Polymer Thermistor		B/			B/	B/	B/	B/
PTC Ceramic Thermistor		2			2	2	2	2
NTC Thermistor		2			2	2	2	2
Trimmer		2		2	2	2	2	2
Varistor	2	2	2	2	2	2	2	2
Resonator/Crystal		2	2	2	2	2		
Attenuator	2	2	2	2	2	2	2	2

A/ moisture soaking to MSL 1 before reflow for plastic packaged SMD capacitors, inductors and attenuators only. If device is incapable of MSL1, can soak at MSL3 before reflow, but parts must be drypacked for shipment to user.

B/ three reflow passes at 260ºC/20 seconds (instead of 10 seconds) onto test boards

C/ Aluminum electrolytics must be allowed to cool after the first and before the second reflow passes

4.3.3 Resistance to Dissolution of Metallization Test

Perform this test per section 4.2.4 of J-STD-002 using a solder dip temperature of 260 +0/-5 C.

Table 4.2

ISSUE	PASSIVE DEVICES
Qualification Requirements	AEC-Q200
Resistance to Dissolution of Metallization	J-STD-002 Section 4.2.4 260+0/-5C

4.3.4 Tin (Sn) Whisker Growth Evaluation

Tin whisker growth is more likely to occur, influenced by complex material and processing conditions, when tin termination plating is used. This is a wearout reliability issue in that these whiskers can grow to contact adjacent terminations to cause false data pulses, intermittent failures and, in extreme circumstances, electrical overstress.

4.3.4.1 Termination Plating

If using tin without an underlayer (e.g., Ni) as the termination plating, it must be deposited in a very clean environment and must display a matte finish. In addition, some studies have shown that a tin plating thickness >7um, a nickel underlayer and/or a postbake at 150^{O}C/1 hour will minimize the likelihood of whisker growth. These conditions have been identified as major factors in minimizing tin whisker growth.

4.3.4.2 Tin Whisker Growth Testing

Suppliers must test for susceptibility to whisker growth during device aging. After each stress, the terminations shall be observed visually using a high power (>50X) microscope. Any termination displaying a whisker filament greater than or equal to 50um in total axial length shall constitute a failure.

Table 4.3 – Tin Whisker Test Conditions

Stress Type	Reference Specification	Test Conditions	Inspection Intervals	Minimum Duration
Temperature Cycling	JESD22 Method A104	T_{MIN} = -55 (+0/-10)^{O}C T_{MAX} = 85 (+10/-0)^{O}C Air-to-air t_{SOAK} = 5 to 10 min. ~3 cycles/hour	500 cycles	1000 cycles
Ambient Temperature/ Humidity Storage		30 +/- 2 ^{O}C 60 +/- 3 %RH	1000 hours	3000 hours
High Temperature/ Humidity Storage		60 +/- 5 ^{O}C 87 +3/-2 %RH	1000 hours	3000 hours

The above inspection intervals and minimum durations are based on experimental data and are given to make data comparisons easier. Total test durations (cycles/hour) are not specified in JESD22 Method A121. Some experimental data suggests that there is an incubation time during which whiskers do not appear. This incubation time depends on lead finish, thickness of the finish and substrate characteristics. If test durations are too short, whiskers will not be observed. For qualification of lead finishes, test duration and inspection intervals will be defined in the qualification plan agreed to by the supplier and user.

4.4 Data Submission Format

Data summary shall be submitted as defined in Appendix 4. The individual user shall submit raw data and histograms upon request. All data and documents (e.g., justification for non-performed test, etc.) shall be maintained by the supplier in accordance with QS-9000 / TS-16949 requirements.

TABLE 1 - QUALIFICATION SAMPLE SIZE REQUIREMENTS					
Stress	**NO.**	**Note**	**Sample Size Per Lot**	**Number of lots**	**Accept on Number failed**
Pre-and Post-Stress Electrical Test	1	G	All qualification parts submitted for testing		0
TEST NOT USED	2	---------	----------		----------
High Temperature Exposure	3	DG	77 Note B	1	0
Temperature Cycling	4	DG	77 Note B	1	0
Destructive Physical Analysis	5	DG	5 Note B	1	0
Moisture Resistance	6	DG	77 Note B	1	0
Humidity Bias	7	DG	77 Note B	1	0
High Temperature Operating Life	8	DG	77 Note B	1	0
External Visual	9	NG	All qualification parts submitted		0
Physical Dimensions	10	NG	30	1	0
Terminal Strength	11	DGL	30	1	0
Resistance to Solvent	12	DG	5	1	0
Mechanical Shock	13	DG	30 Note B	1	0
Vibration	14	DG			
Resistance to Solder Heat	15	DGC	30	1	0
Thermal Shock	16	DG	30	1	0
ESD	17	D	15	1	0

TABLE 1 - QUALIFICATION SAMPLE SIZE REQUIREMENTS (cont)					
Stress	**NO.**	**Note**	**Sample Size Per Lot**	**Number of lots**	**Accept on Number failed**
Solderability	18	DC	15 each condition	1	0
Electrical Characterization	19	NG	30 Note A	3	0
Flammability	20	D	Present certificate of compliance		
Board Flex	21	DS	30	1	0
Terminal Strength (SMD)	22	DS	30	1	0
Beam Load	23	DG	30	1	0
Flame Retardance	24	DG	30	1	0
Rotation Life	25	DG	30	1	0
TEST NOT USED	26	--------	----------	----------	----------
Surge Voltage	27	DG	30	1	0
TEST NOT USED	28	--------	----------	----------	----------
Salt Spray	29	DG	30	1	0
Electrical Transient Conduction	30	DG	30	1	0

LEGEND FOR TABLE 1

Note:
- A For parametric verification data, sometimes circumstances may necessitate the acceptance of only one lot by the user. Should a subsequent user decide to use a previous user's qualification approval, it will be the subsequent user's responsibility to verify that an acceptable number of lots was used.
- B Where generic (family) data is provided in lieu of component specific data, 3 lots are required.
- C The solderability (test #18) and resistance to solder heat (test #15) tests are still required to be performed on Pb-free product for backward compatibility with Pb processes.
- D Destructive test, devices are not to be reused for qualification or production.
- G Generic data allowed. See Section 2.3.
- H Required for hermetic packaged devices only.
- L Required for leaded devices only.
- N Nondestructive test, devices can be used to populate other tests or they can be used for production.
- S Required for surface mount devices only.

TABLE 2 - TABLE OF METHODS REFERENCED TANTALUM & CERAMIC CAPACITORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 2.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	Unpowered 1000 hours @ T=150°C (Ceramics). 1000 hours @ T=125°C (Tantalums). Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 Cycles (-55°C to +125°C) Measurement at 24±2 hours after test conclusion.
Destructive Physical Analysis	5	EIA-469	10ea X 3 lots Note: Only applies to SMD Ceramics. Electrical Test not required.
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85% RH. Note: Ceramics only - Specified conditions: Rated Voltage and 1.3 to 1.5 volts. Add 100Kohm resistor. Tantalums - Rated Voltage Only. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	Condition D Steady State T_A=125°C. 2/3 rated for Tantalum caps Full rated for Ceramic caps Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device specification. Note: User(s) and Suppliers spec. Electrical Test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: Ceramics: A (454 g), C (227 g), E (1.45 kg-mm). Tantalums: A (2.27 kg), C (227 g), E (1.45 kg-mm).
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Add Aqueous wash chemical - OKEM Clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213 SMD: Condition F LEADED: Condition C
Vibration	14	MIL-STD-202 Method 204	5 g's for 20 min., 12 cycles each of 3 orientations Note: Use 8"X5" PCB .031" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any

TABLE 2 - TABLE OF METHODS REFERENCED TANTALUM & CERAMIC CAPACITORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
			secure point. Test from 10-2000 Hz.

TABLE 2 - TABLE OF METHODS REFERENCED TANTALUM & CERAMIC CAPACITORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples Note: Single Wave Solder - Procedure 2 for SMD. Procedure 1 for Leaded with solder within 1.5mm of device body.
Thermal Shock	16	MIL-STD-202 Method 107	-55°C/+125°C. Note: Number of cycles required-300, Maximum transfer time-20 seconds, Dwell time-15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical Test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
TEST NOT USED	20	----------	----------
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (min) for all except 3mm for Class 1.
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: Force of 1.8kg for 60 seconds.
Beam Load Test	23	AEC-Q200-003	Ceramics Only
TEST NOT USED	24	----------	----------
TEST NOT USED	28	----------	----------

NOTE: Pre-stress electrical tests also serve as electrical characterization
Interval measurements for 1000 hour tests required at 250 and 500 hrs.

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TABLE 2A - Ceramic/Tantalum Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
5. Destructive Physical Analysis
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
21. Board Flex
22. Terminal Strength (SMD)
23. Beam Load Test

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	21	22	23					
MATERIAL																									
Binder Material		●	●									●		●											
Dielectric Change	●	●	●		●	●			●	●	●	●		●	●		B	C		●					
Electrode Attach	●	●				●							C	●			B	C	●						
Electrode Material	●	●	●		●	●			●	●		●		●	●		B								
Encapsulation		●		●	●		●	●		●															
Lead Material		●	●			●	●		●			●	●			●	B								
PROCESS																									
Dicing	●	●		●	●		●	●		●	●						B			C					
Electrode Apply	C				C								C	C	C		BC	C							
Firing Profile		●	●			●								●	●		B			C					
Lamination/Press Technique			●		●								●	●			B	●		C					
Powder Particle Size		●			●								●		●		B	●							
Screening/Printing						C					C				C		BC			C					
Termination Process	●	●	●	●	●	●	●	●	●	●	●	●	●			●	B	●	●						
DESIGN																									
Electrode Thickness	●	●	●			●		●			●	●		●	●		B								
Layer Thickness	●	●	●		●	●		●	●		●			●	●		B			C					
Lead Diameter		●		●	●	●	●	●	●			●													
Number of Layers		C	C		C	C		C			C			C	C		BC			C					
Termination Area	●			●			●	●				●						●	●						
Terminal Interface	●	●	●	●	●	●			●		●	●	●				B	●	●						
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	B	●	●	C					
Material Suppliers	●	●	●	●	●	●			●	●	●	●	●	●	●	●	B	●	●	C					
New/Modified Mfg. Equipment		●		●	●	●		●	a			●			●	●	B			C					

a = termination equipment only B = comparative data (unchanged vs. Changed) required c = Ceramics only

TABLE 3 - TABLE OF METHODS REFERENCED ALUMINUM ELECTROLYTIC CAPACITORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 3.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated operating temperature (e.g. 85°C part can be stored for 1000 hrs at 85°C. The same applies for 105°C & 125°C). Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 cycles (-40°C to 105°C) Note: If 85°C or 125°C part the 1000 cycles will be at that temperature rating. Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Rated Voltage. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	Note: 1000 hrs @ 105°C. If 85°C or 125°C part will be tested at that temperature. Rated Voltage applied. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device detail specification. Note: User(s) and Suppliers spec. Electrical Test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (454 g), C (227 g), E (1.45 kg-mm)
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Also aqueous wash chemical - OKEM clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213. Condition C
Vibration	14	MIL-STD-202 Method 204	5g's for 20 minutes 12 cycles each of 3 orientations. Note: Use 8"X5" PCB .031" thick with 7 secure points on one 8" side and 2 secure points on corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.

TABLE 3 - TABLE OF METHODS REFERENCED ALUMINUM ELECTROLYTIC CAPACITORS			
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B no pre-heat of samples. Note: Single Wave Solder. Procedure 1 with solder within 1.5mm of device body for Leaded and 0.75mm for SMD. SMD – remove carrier.
Thermal Shock	16	MIL-STD-202 Method 107	Condition A. If 125°C part use -55°C/+125°C. Note: Number of Cycles: 300; Max. transfer time: 20 seconds; Dwell time: 15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical Test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3 c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 Acceptable
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (Min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: A force of 1.8kg for 60 seconds.
Surge Voltage	27	AEC-Q200-007	
TEST NOT USED	28	----------	----------
TEST NOT USED	30	----------	----------

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval measurements for 1000 hour tests required at 250 and 500 hrs.

TABLE 3A - Electrolytic Capacitor Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)
27. Surge Voltage

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 3	3	4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	27					
MATERIAL																									
End Seal		●	●	●	●	●	●		●				●				●								
Housing		●	●				●			●			●				●								
Sleeving		●	●		●	●	●		●				●				●								
Lead/Termination								●			●	●			●	B		●	●						
PROCESS																									
Curing		●		●	●		●						●	●		B				●					
Impregnation method	●	●			●									●		B				●					
Terminal Attach		●						●		●		●	●			B		●	●						
Winding		●			●						●					B									
DESIGN																									
Electrolyte Change	●	●			●								●	●		B				●					
Foil Design		●			●									●		B				●					
Insulation Change		●			●									●		B				●					
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	B	●	●	●	●					
Material Suppliers	●	●	●	●				●	●	●	●	●	●		●	B	●	●	●						
New/Modified Mfg. Equipment		●			●		●	●		●	●			●		B				●					

B = comparative data (unchanged vs. Changed) required

TABLE 4 - TABLE OF METHODS REFERENCED FILM CAPACITORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 4.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated operating temperature (e.g. 85°C part can be stored for 1000 hrs at 85C. The same applies for 100°C & 125°C parts.). Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 cycles (-55°C to 85°C) Note: If 100°C or 125°C part the 1000 cycles will be at that temperature rating. Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 40°C/93%RH. Rated Voltage. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	1000 hours T_A=85°C, Note: Condition D (1000 hrs) If 100°C or 125°C the 1000 hrs. will be at that temperature. Metallized Film: 125% of rated voltage at 85°C. 100% of rated voltage above 85°C. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device specification. Note: User(s) and Suppliers spec. Electrical Test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (2.27 kg), C (227 g), E (1.45 kg-mm)
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Also aqueous wash chemical - OKEM clean or equivalent. Do not use banned solvents
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213. Condition C
Vibration	14	MIL-STD-202 Method 204	5g's for 20 minutes, 12 cycles each of 3 orientations Use 8"X5" PCB, .031" thick. 7 secure points on one 8" side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.

TABLE 4 - TABLE OF METHODS REFERENCED FILM CAPACITORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Note: For SMD use Procedure 2; For Leaded use Procedure 1 with solder within 1.5mm of device body.
Thermal Shock	16	MIL-STD-202 Method 107	-55°C/+85°C. Note: Number of Cycles: 300; If 100°C or 125°C part the 300 cycles will be at that temperature rating. Maximum Transfer Time: 20 seconds; Dwell Time: 15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical Test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 are acceptable. Electrical Test not required.
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: A force of 1.8kg for 60 seconds.
TEST NOT USED	26	----------	----------
TEST NOT USED	28	----------	----------
TEST NOT USED	30	----------	----------

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval Measurements for 1000 hour tests required at 250 hrs. and 500 hrs.

TABLE 4A - Film Capacitor Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 4	3	4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22						
MATERIAL																									
Epoxy	●	●	●	●	●	●	●		●	●	●		●				●								
Housing		●		●	●	●	●	●		●	●				●										
Lead/Termination			●				●	●		●		●			●	B		●	●						
PROCESS																									
Epoxy Fill	●	●		●	●	●			●																
Terminal attach		●	●		●			●	●							B		●	●						
Winding	●				●									●		B									
DESIGN																									
Foil Design		●			●									●		B									
Insulation Change		●			●									●		B									
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	B	●	●	●						
Material Suppliers	●	●	●		●			●	●		●	●	●		●		●		●						
New/Modified Mfg. Equipment		●	●		●			●					●	●		B			●						

B = comparative data (unchanged vs. Changed) required

TABLE 5 - TABLE OF METHODS REFERENCED MAGNETICS (INDUCTORS/TRANSFORMERS)			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 5.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated operating temperature (e.g. 125°C part can be stored for 1000 hrs. @ 125°C. The same applies for 105°C and 85°C. Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 cycles (-40°C to +125°C). Note: If 85°C part or 105°C part the 1000 cycles will be at that temperature. Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Unpowered. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-PRF-27	1000 hrs. @ 105°C. If 85°C or 125°C part will be tested at that temperature. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device detail specification. Note: User(s) and Suppliers spec. Electrical Test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (910 g), C (1.13 kg), E (1.45 kg-mm)
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Add Aqueous wash chemical. OKEM Clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213. Condition C
Vibration	14	MIL-STD-202 Method 204	5g's for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8"X5" PCB, .031" thick, 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.

TABLE 5 - TABLE OF METHODS REFERENCED MAGNETICS (INDUCTORS/TRANSFORMERS)			
Stress	**NO.**	**Reference**	**Additional Requirements**
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples. Note: Single Wave Solder - Procedure 2 for SMD and Procedure 1 for Leaded with solder within 1.5mm of device body.
Thermal Shock	16	MIL-STD-202 Method 107	-40°C/+125°C. Note: Number of cycles required is 300. Maximum transfer time is 20 seconds. Dwell time is 15 minutes. Below 125°C use Condition A for maximum temperature. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical Test not required. Magnification 50X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 Acceptable
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (Min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: Force of 1.8kg for 60 seconds.
TEST NOT USED	26	----------	----------
TEST NOT USED	28	----------	----------
TEST NOT USED	30	----------	----------

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval measurements for 1000 hour tests required at 250 and 500 hrs.

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TABLE 5A - Inductive Products Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 5	3	4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22						
MATERIAL																									
Bobbin material	●	●		●	●	●				●			●				●								
Core material		●			●	●				●			●			B	●								
Insulation material	●	●		●	●	●			●			●	●	a		B	●								
Lead material					●	●		●			●	●			●			●	●						
Mold material	●	●	●	●	●	●			●	●			●			B	●								
Solder material		●				●		●		●	●		●		●			●	●						
Wire/foil material			●	●	●	●								●		B		●	●						
PROCESS																									
Insulation strip			●			●			●			●													
Lead prep/plating		●				●		●			●	●	●		●			●	●						
Terminal Attach		●	●			●		●		●	●	a	●		●										
Marking						●			●																
Molding	●	●		●	●	●	●		●	●			●			B	●								
Soldering		●				●		●			●		●		●			●	●						
Winding - Insulation				●	●				●			●		a		B									
Winding - Wire			●		●	●										B									
DESIGN																									
Bobbin		●				●	●			●			●	●		B									
Core		●				●	●			●	●		●			B									
Insulation system				●	●	●	●		●			●		a		B	●								
Lead						●	●	●			●	●		●	●			●	●						
Mold		●	●			●	●		●	●			●			B									
Wire/foil		●				●	●						●			B		●	●						
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●		●			●				●	●			B			●						
Material Suppliers		●	●			●	●	●					●			B									
Process Control Change						●	●																		

a = Multilayer only

B = comparative data (unchanged vs. Changed) required

TABLE 6 - TABLE OF METHODS REFERENCED NETWORKS (R-C/C/R)			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 6.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated temperature (e.g. 85°C part can be stored for 1000 hrs. at 85°C. The same applies for 125°C part. Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 cycles (-55°C to 125°C) Note: If 85C part the 1000 cycles will be at that temperature. Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Capacitor Networks - Rated Voltage Resistor Networks - 10% Rated Power. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	1000 hrs. T_A=85°C Note: If 125°C part the 1000 hrs. will be at that rated temperature. Rated Voltage. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device detail specification. Note: User(s) and Supplier spec. Electrical test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Condition: A (227 g), C (227 g)
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Add Aqueous wash chemical – OKEM Clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213. Condition C
Vibration	14	MIL-STD-202 Method 204	5g's for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8"X5" PCB .031" thick, 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples. Note: Single Wave Solder - Procedure 2 for SMD and Procedure 1 for Leaded with solder within 1.5mm of device body.

TABLE 6 - TABLE OF METHODS REFERENCED NETWORKS (R-C/C/R)			
Stress	**NO.**	**Reference**	**Additional Requirements**
Thermal Shock	16	MIL-STD-202 Method 107	Condition A If 125°C part use -55°C/+125°C. Note: Number of cycles: 300; Max. transfer time: 20 seconds; Dwell time: 15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 acceptable
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (Min) for all except 3mm for Class 1.
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: Force of 1.8kg for 60 seconds.
TEST NOT USED	26	----------	----------
TEST NOT USED	28	----------	----------
Salt Spray	29	MIL-STD-202 Method 101	Test condition B

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval measurements for 1000 hour tests required at 250 and 500 hours.

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TABLE 6A/7A - Networks and Resistors Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)
24. Flame Retardance
29. Salt Spray

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Tables 6 and 7	**3**	**4**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**24**	**29**				
MATERIAL																									
Ink/Wire Material	●	●			●			W					●	F		B		●	●	R					
Package	●	●	●	●		●	●	●	●		●		●	●			●	●	●	R					
Passivation	●	●	●	●	●				●				●				●			R	N				
Substrate Material		●	●	●	●			●				●	●		●	B		●	●						
PROCESS																									
Ink Fire		●			●			R								B									
Ink Print	●	●			●			R					●			B		R	R	R					
Laser Trim				●	●											B									
Lead Form				●		●	●	●							●	B					N				
Termination Attach				●				●		●		●				B					N				
Marking						●			●																
Molding	●	●	●	●		●	●	●	●		●		●	●			●	●	●	R					
DESIGN																									
Package	●	●	●	●		●	●	●	●		●	●	●	●	●		●	●	●	R					
Passivation	●	●	●	●	●				●				●				●			R	N				
Res/Cap Tolerance	●	●			●							●	●	●		B									
Res/Cap Value	●	●			●							●	●	●		B				R					
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●	●			●	●	●		B		●	●	R	N				
Material Suppliers		●	●				●	●	●			●	●	●		B	●			R	N				
New/Modified Mfg. Equipment		●	●		●								●	●		B									

R = Resistors Only
N = Networks Only
F = Film products only
W = Wirewound products only
B = comparative data (unchanged vs. Changed) required

TABLE 7 - TABLE OF METHODS REFERENCED RESISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 7.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. @ T=125°C. Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 Cycles (-55°C to +125°C) Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Note: Specified conditions: 10% of operating power. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	Condition D Steady State T_A=125°C at rated power. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Electrical test not required. Inspect device construction, marking and workmanship.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device detail specification. Note: User(s) and Suppliers spec. Electrical test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (2.27 kg), C (227 g), E (1.45 kg-mm)
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Add Aqueous wash chemical - OKEM Clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213. Condition C
Vibration	14	MIL-STD-202 Method 204	5 g's for 20 min., 12 cycles each of 3 orientations. Note: Use 8"X5" PCB .031" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples. Note: Single Wave Solder - Procedure 2 for SMD and Procedure 1 for Leaded with solder within 1.5mm of device body.

TABLE 7 - TABLE OF METHODS REFERENCED RESISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Thermal Shock	16	MIL-STD-202 Method 107	-55°C/+125°C. Note: Number of cycles required-300, Maximum transfer time-20 seconds, Dwell time-15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 are acceptable. Electrical test not required.
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (Min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: Force of 1.8kg for 60 seconds.
Flame Retardance	24	AEC-Q200-001	
TEST NOT USED	28	----------	----------

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval measurements for 1000 hour tests required at 250 hrs and 500 hrs.

TABLE 8 - TABLE OF METHODS REFERENCED THERMISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 8.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated operating temperature (e.g. 85°C part can be stored for 1000 hrs at 85°C, same applies for 125°C part. Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 Cycles (-55°C to +125°C) Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. 10% Rated Power. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	1000 hrs. T=125°C Note: If 85°C part 1000 hrs. will be at that temperature. Rated power at temperature - steady state. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device specification.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (2.27 kg), C (227 g).
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Add Aqueous wash chemical - OKEM Clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202-213	Figure 1 of Method 213 SMD: Condition F LEADED: Condition C
Vibration	14	MIL-STD-202 Method 204	5 g's for 20 min., 12 cycles each of 3 orientations Note: Use 8"X5" PCB .031" thick. 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples. Note: Single Wave Solder - Procedure 2 for SMD and Procedure 1 for Leaded with solder within 1.5 mm

TABLE 8 - TABLE OF METHODS REFERENCED THERMISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
			of part body.

TABLE 8 -TABLE OF METHODS REFERENCED THERMISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Thermal Shock	16	MIL-STD-202 Method 107	-55°C/+125°C. Note: Number of cycles required is 300. Maximum transfer time is 20 seconds. Dwell time is 15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 are acceptable. Electrical test not required.
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (Min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: Force of 1.8kg for 60 seconds.
TEST NOT USED	26	----------	----------
TEST NOT USED	28	----------	----------
TEST NOT USED	30	----------	----------

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval measurements for 1000 hour tests required at 250 hrs. and 500 hrs.

TABLE 8A - Thermistor Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 8	3	4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22						
MATERIAL																									
Ink Material	●	●		●	●									●		B									
Protective Coat	●	●	●										●												
Substrate Material										●		●	●		●		●								
PROCESS																									
Lead Form			●			●	●	●								B		●	●						
Marking						●			●																
Molding	●	●				●	●		●		●	●			●		●								
Termination Attach			●	●	●			●		●				●	●	B		●	●						
DESIGN																									
Package	●	●	●	●	●	●	●	●	●	●	●	●	●		●		●								
Thermistor Value	●	●			●									●		B									
Thermistor Tolerance	●	●			●							●		●		B									
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●		●	●	●	●		●	●	●	●	●	●	B	●	●	●						
Material Suppliers		●	●		●			●	●			●	●		●	B	●	●	●						

B = comparative data (unchanged vs. Changed) required

TABLE 9 - TABLE OF METHODS REFERENCED TRIMMER CAPACITORS/RESISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 9.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated operating temperature (e.g. 85°C part can be stored for 1000 hrs. at 85°C and the same applies for 125°C). Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 Cycles (-55°C to 85°C) Note: If 125°C part the 1000 cycles will be at that temperature rating. Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Capacitive Trimmers - Rated Voltage Resistive Trimmers - 10% Rated Power. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	1000 hrs T_A=85°C Note: If 125°C part it will be tested at that temperature. Rated Voltage for trimmer caps. Rated power at temperature for trimmer resistors. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device detail specification. Note: User(s) and Supplier spec. Electrical test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (227 g), C (227 g)
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Add Aqueous wash chemical - OKEM Clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213 SMD: Condition F LEADED: Condition C

TABLE 9 - TABLE OF METHODS REFERENCED TRIMMER CAPACITORS/RESISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Vibration	14	MIL-STD-202 Method 204	5 g's for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8"X5" PCB .031" thick, 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples. Note: Single Wave solder - Procedure 1 with solder within 1.5 mm of device body for Leaded. Procedure 1 except 230°C and immerse only to level to cover terminals for SMD.
Thermal Shock	16	MIL-STD-202 Method 107	Condition A. If 125°C part use -55°C/+125°C. Note: Number of Cycles: 300; Max. Transfer time: 20 seconds; Dwell time: 5 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 are acceptable. Electrical test not required.
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (Min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: A force of 1.8kg for 60 seconds.
TEST NOT USED	23	----------	----------
TEST NOT USED	24	----------	----------
Rotation Life	25	MIL-STD-202 Method 206	Condition A

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval measurements for 1000 hour tests required at 250 hrs. and 500 hrs.

TABLE 9A - Trimmers Capacitors/Resistors Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)
25. Rotation Life

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 9	3	4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	25					
MATERIAL																									
Element Material		●	●											●		B				●					
Housing Material		●			●	●	●						●												
Substrate		●		●						●			●												
Termination Material		●			●		●	●	●	C	●	●	●		●			●	●						
Washer	●	●	●						●						●					●					
PROCESS																									
Brush Attach		●		●							●		●			B				●					
Termination Attach		●			●			●				●	●					●	●						
DESIGN																									
Element		●	●											●		B				●					
Housing	●	●			●	●	●		●				●				●								
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	B	●	●	●	●					
Material Suppliers		●					●			C					●										

C = Capacitive Trimmers only B = comparative data (unchanged vs. Changed) required

TABLE 10 - TABLE OF METHODS REFERENCED VARISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 10.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. @ T=150°C. Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 cycles (-40°C to 125°C) Electrical test before and after TC. Note: If 85°C part the 1000 cycles will be at that temperature rating. Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Bias at 85% (+5%/-0%) of rated Varistor voltage (1 mA) Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	1000 hrs. T_A=125°C. Note: If 85°C part 1000 hrs will be at that temperature. Bias at 85% (+5%/-0%) of rated Varistor voltage (ma) Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device detail specification. Note: User(s) and Supplier spec. Electrical test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (2.27 kg), C (227 g)
Resistance to Solvents	12	MIL-STD-202 Method 215	Also aqueous wash chemical - OKEM Clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213 SMD: Condition F LEADED: Condition C
Vibration	14	MIL-STD-202 Method 204	5 g's for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8"X5" PCB .031" thick with 7 secure points on one 8" side and 2 secure points on corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.

TABLE 10 - TABLE OF METHODS REFERENCED VARISTORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples. Note: Single Wave solder - Procedure 2 for SMD. Procedure 1 with solder within 1.5 mm of device body for Leaded.
Thermal Shock	16	MIL-STD-202 Method 107	-55°C/+125°C. Note: Number of Cycles required is 300. Maximum transfer time is 20 seconds. Dwell time is 15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical test not required. Magnification 50 X. Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 are acceptable. Electrical test not required.
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (Min.)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: Force of 1.8kg for 60 seconds.
TEST NOT USED	26	----------	----------
TEST NOT USED	28	----------	----------
Electrical Transient Conduction	30	ISO-7637-1	Test pulses 1 to 3

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval measurements for 1000 hour tests required at 250 hrs and 500 hrs.

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TABLE 10A - Varistors Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)
30. Electrical Transient Conduction

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 10	3	4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	30					
MATERIAL																									
Coating Material	●	●	●			●			●	●	●		●				●								
Electrode Attach	●	●			●			●				●	●			B		●	●	●					
Element Material	●	●			●					●			●	●		B				●					
Passivation		●	●										●					●							
Termination	●	●			●			●				●	●		●	B		●	●	●					
PROCESS																									
Coating Dip/Cure	●	●	●			●	●		●				●				●								
Dicing		●		●		●	●						●			B		●	●	●					
Lead Forming	●		●	●			●	●			●	●	●		●	B									
Marking	●					●			●																
Sintering	●	●	●		●								●	●		B				●					
Termination Attach	●	●			●		●	●			●	●	●			B		●	●	●					
Termination Plating	●	●			●		●	●				●	●		●	B		●	●						
DESIGN																									
Element Size		●	●		●					●	●		●	●		B				●					
Grain Boundary Size			●		●									●		B				●					
Grain Size					●											B				●					
Layer - Number of		●	●		●						●		●							●					
Layer - Thickness			●		●											B		●	●	●					
Package Size		●	●		●	●	●	●		●	●		●	●				●		●					
Passivation Thickness		●	●		●					●			●			B									
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●		●	●	●	●	●	●	B		●	●	●					
Material Suppliers	●	●	●		●			●			●	●		●	●	B		●	●	●					
New/Modified Mfg. Equipment		●	●		●			●			●			●		B				●					

B = comparative data (unchanged vs. Changed) required

TABLE 11 - TABLE OF METHODS REFERENCED QUARTZ CRYSTALS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 11.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated operating temperature (e.g. 85°C part can be stored for 1000 hrs at 85°C. The same applies for 125°C). Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 cycles (-40°C to 125°C) Note: If 85°C part the 1000 cycles will be at that temperature rating. Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Rated V_{DD} applied with 1 MΩ and inverter in parallel, 2X crystal C_L capacitors between each crystal leg and GND. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	Note: 1000 hrs @ 125°C. If 85C part will be tested at that temperature. Rated V_{DD} applied with 1 MΩ and inverter in parallel, 2X crystal C_L capacitors between each crystal leg and GND. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device detail specification. Note: User(s) and Suppliers spec. Electrical Test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (227 g), C (227 g).
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Also aqueous wash chemical - OKEM clean or equivalent. Do not use banned solvents.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213. Condition C
Vibration	14	MIL-STD-202 Method 204	5g's for 20 minutes 12 cycles each of 3 orientations. Note: Use 8"X5" PCB .031" thick with 7 secure points on one 8" side and 2 secure points on corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.

TABLE 11 - TABLE OF METHODS REFERENCED QUARTZ CRYSTALS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples. Note: Single Wave solder - Procedure 1 with solder within 1.5 mm of device body for Leaded. Procedure 1 except 230°C and immerse only to level to cover terminals for SMD.
Thermal Shock	16	MIL-STD-202 Method 107	Condition A. If 125°C part use -55°C/+125°C. Note: Number of Cycles: 300; Max. transfer time: 20 seconds; Dwell time: 5 minutes. Air-Air.
TEST NOT USED	17	----------	----------
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical Test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 Acceptable
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (Min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: A force of 1.8kg for 60 seconds.
TEST NOT USED	27	----------	----------
TEST NOT USED	28	----------	----------
TEST NOT USED	30	----------	----------

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval measurements for 1000 hour tests required at 250 and 500 hrs.

TABLE 11A- Quartz Crystal Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 11	3	4	6	7	8	9	10	11	12	13	14	15	16	18	19	20	21	22							
MATERIAL																									
Quartz Blank	●	●			●					●	●		●		B		●								
Base		●		●		●	●		●	●	●						●	●							
Lead/Termination		●				●	●	●	●		●	●		●	B		●	●							
Glass Seal	●	●	●	●	●	●		●	●	●	●	●	●		B		●	●							
Can/Cap		●		●		●	●		●	●	●						●								
Blank Support		●			●					●	●		●		B		●								
Overmold	●	●	●			●	●		●	●	●	●	●			●	●	●							
Case Sealing	●	●		●		●			●	●	●	●	●		B	●	●								
Electrode	●	●			●						●		●												
Insulator	●	●	●			●	●		●		●	●	●		B	●	●								
PROCESS																									
Quartz Blank		●			●					●	●		●		B		●								
Base Assembly	●	●		●		●	●	●		●	●	●	●	●			●	●							
Blank Etch/Clean															B										
Electrode Formation		●			●						●				B		●								
Auto Trim										●	●				B		●								
Bond/Anneal Blank	●	●			●					●	●		●		B		●								
Cap/Can Attach	●	●		●	●	●	●			●	●		●		B		●								
Overmolding		●	●			●	●			●	●		●		B	●	●	●							
Marking						●			●																
Aging										●	●		●		B		●								
DESIGN																									
Quartz Blank		●								●	●				B		●								
Base	●	●		●		●	●	●		●	●		●				●	●							
Lead/Termination		●				●	●	●		●	●	●	●	●	B		●	●							
Can/Cap		●	●	●		●	●			●	●		●		B		●								
Blank Support		●			●					●	●		●		B		●								
Package (Molded)		●	●			●	●	●	●	●	●	●	●		B	●	●	●							
Insulator						●	●		●																
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●	●	●	●	●	●	●	B	●	●	●							
Material Suppliers		●	●		●	●	●	●	●	●	●		●	●	B	●	●	●							
Process Control Change						●	●																		

B = comparative data (unchanged vs. Changed) required

TABLE 12 - TABLE OF METHODS REFERENCED CERAMIC RESONATORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 12.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated operating temperature (e.g. 85°C part can be stored for 1000 hrs at 85°C. The same applies for 125°C parts.). Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 cycles (-55°C to 85°C) Note: If 125°C part the 1000 cycles will be at that temperature rating. Measurement at 24±2 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered. Measurement at 24±2 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Rated V_{DD} applied with 1 MΩ and inverter in parallel, 2X resonator C_L capacitors between each resonator leg and GND. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	1000 hours T_A=85°C, Note: Condition D (1000 hrs) If 125°C the 1000 hrs. will be at that temperature. Rated V_{DD} applied with 1 MΩ and inverter in parallel, 2X resonator C_L capacitors between each resonator leg and GND. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device specification. Note: User(s) and Suppliers spec. Electrical Test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (2.27 kg), C (227 g)
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Also aqueous wash chemical - OKEM clean or equivalent. Do not use banned solvents
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213. Condition C

TABLE 12 - TABLE OF METHODS REFERENCED CERAMIC RESONATORS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Vibration	14	MIL-STD-202 Method 204	5g's for 20 minutes, 12 cycles each of 3 orientations Use 8"X5" PCB, .031" thick. 7 secure points on one 8" side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Condition B No pre-heat of samples. Note: Single Wave solder - Procedure 1 with solder within 1.5 mm of device body for Leaded. Procedure 1 except 230°C and immerse only to level to cover terminals for SMD.
Thermal Shock	16	MIL-STD-202 Method 107	Condition A. If 125°C part test at -55°C/125°C. Note: Number of Cycles: 300; Maximum Transfer Time: 20 seconds; Dwell Time: 15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical Test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
TEST NOT USED	20	----------	----------
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: A force of 1.8kg for 60 seconds.
TEST NOT USED	26	----------	----------
TEST NOT USED	28	----------	----------
TEST NOT USED	30	----------	----------

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval Measurements for 1000 hour tests required at 250 hrs. and 500 hrs.

TABLE 12A - Ceramic Resonator Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
21. Board Flex
22. Terminal Strength (SMD)

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 12	3	4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	21	22							
MATERIAL																									
Ceramic Element	●	●	●		●			●		●	●		●			B									
Inner Electrode	●	●	●		●			●		●	●		●	●											
Epoxy Resin Overcoat	●	●		●	●	●	●	●	●																
Outer Electrode		●	●			●	●	●	●		●	●	●	●	●		●	●							
Wax						●										B									
Terminal Solder		●				●									●		●	●							
Element/Lead Attach	●	●	●		●			●		●	●	●	●	●		B									
Case	●	●	●		●	●	●		●	●	●	●	●				●	●							
Case Adhesive/Seal	●	●	●		●	●	●	●	●	●	●	●	●				●	●							
Capacitor	●	●	●		●			●		●	●	●	●	●		B	●	●							
PROCESS																									
Ceramic Blank		●			●			●		●	●		●			B	●	●							
Lapping		●						●		●	●		●			B	●	●							
Electroding		●			●			●		●	●		●	●		B	●	●							
Cutting								●		●	●		●			B	●	●							
Annealing					●			●		●	●		●			B	●	●							
Polarize/Freq. Adjust														●		B									
Element/Lead Attach		●			●			●		●	●			●		B	●	●							
Adhesive/Epoxy Seal		●		●	●	●				●	●						●								
Epoxy Dip & Cure			●		●	●	●	●	●																
Wax Application						●	●																		
Terminal Solder	●	●	●		●	●	●	●							●		●	●							
Marking						●			●																
DESIGN																									
Ceramic Element		●			●		●			●	●		●			B	●								
Electrode/Capacitor		●			●			●		●	●		●	●		B	●	●							
Case		●	●		●	●	●			●	●		●				●	●							
Termination		●			●	●		●		●	●		●		●		●	●							
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	B	●	●							
Material Suppliers		●	●		●	●	●	●	●	●	●		●		●	B	●	●							
New/Modified Mfg. Equipment						●	●																		

B = comparative data (unchanged vs. Changed) required

TABLE 13 - TABLE OF METHODS REFERENCED FERRITE EMI SUPPRESSORS/FILTERS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 13.
TEST NOT USED	2	----------	----------
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108	1000 hrs. at rated operating temperature (e.g. 85°C part can be stored for 1000 hrs at 85°C. The same applies for 125°C parts.). Unpowered. Measurement at 24±2 hours after test conclusion.
Temperature Cycling	4	JESD22 Method JA-104	1000 cycles (-55°C to 85°C) Note: If 125°C part the 1000 cycles will be at that temperature rating. Measurement at 24±2 hours after test conclusion.
Destructive Physical Analysis	5	EIA-469	10ea X 3 lots. Electrical Test not required.
TEST NOT USED	6	----------	----------
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85%RH. Apply Maximum rated Voltage and current. Measurement at 24±2 hours after test conclusion.
Operational Life	8	MIL-STD-202 Method 108	1000 hours T_A=85°C, Note: If 125°C the 1000 hrs. will be at that temperature. Rated I_L applied. Measurement at 24±2 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical Test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the applicable device specification. Note: User(s) and Suppliers spec. Electrical Test not required.
Terminal Strength (Leaded)	11	MIL-STD-202 Method 211	Test leaded device lead integrity only. Conditions: A (910g), C (1.13kg) , E (1.45 Kg-mm)
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Also aqueous wash chemical - OKEM clean or equivalent. Do not use banned solvents
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213. SMD: Condition F Leaded: Condition C
Vibration	14	MIL-STD-202 Method 204	5g's for 20 minutes, 12 cycles each of 3 orientations Use 8"X5" PCB, .031" thick. 7 secure points on one 8" side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2000 Hz.
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Note: Condition B No pre-heat of samples. Note: Single Wave solder - for SMD use Procedure 2; For Leaded use Procedure 1.

TABLE 13 - TABLE OF METHODS REFERENCED FERRITE EMI SUPPRESSORS/FILTERS			
Stress	**NO.**	**Reference**	**Additional Requirements**
Thermal Shock	16	MIL-STD-202 Method 107	Condition A. If 125°C part test at -55°C/125°C. Note: Number of Cycles: 300; Maximum Transfer Time: 20 seconds; Dwell Time: 15 minutes. Air-Air.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical Test not required. Magnification 50 X. Conditions: Leaded: Method A @ 235°C, category 3. SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C category 3. c) Method D category 3 @ 260°C.
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V-0 or V-1 are acceptable. Electrical Test not required.
Board Flex	21	AEC-Q200-005	Appendix 2 Note: 2mm (min)
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: A force of 1.8kg for 60 seconds.
TEST NOT USED	26	----------	----------
Electrical Transient Conduction	30	ISO-7636-1	Test pulses 1 to 3

NOTE: Pre-stress electrical tests also serve as electrical characterization.
Interval Measurements for 1000 hour tests required at 250 hrs. and 500 hrs.

TABLE 13A - Ferrite EMI Suppressor/ Filter Process Change Qualification Guidelines for the Selection of Tests

3. High Temperature Exposure (Storage)
4. Temperature Cycling
5. Destructive Physical Analysis
7. Biased Humidity
8. Operational Life
9 External Visual
10. Physical Dimension
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. Electrostatic Discharge (ESD)
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex
22. Terminal Strength (SMD)
30. Electrical Transient Conduction
31. Shear Strength

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 13	3	4	5	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	30	31				
MATERIAL																									
Binder Material		●									●		●			B									
Dielectric	●	●	●	●				●		●	●		●	●		B		●							
Terminal Interface	●	●	●	●						●	●		●	●		B		●							
Conductor Material	●	●	●	●	●			●			●		●			B		●							
Encapsulation			●			●	●		●			●	●												
Lead/Termination		●				●	●	●			●	●			●	B			●						
PROCESS																									
Dicing	●	●		●		●	●		●	●						B	●								
Conductor Apply	●			●	●							●	●	●		B		●							
Electrode Formation		●	●		●									●		B				●					
Firing Profile		●	●										●	●		B		●		●					
Lamination Press			●	●								●	●			B		●							
Powder Particle Size		●		●								●		●		B		●							
Screen Printing		●												●		B									
Termination Process	●	●	●	●		●	●	●		●	●	●			●	B		●	●						
DESIGN																									
Conductor Thickness	●	●	●							●			●	●		B									
Lead/Term. Thickness		●				●	●	●			●							●	●		●				
Number of Layers		●	●	●			●						●	●		B		●							
Termination Area		●				●	●				●							●	●		●				
Terminal Interface	●	●	●	●					●	●	●	●	●	●		B		●	●	●					
MISCELLANEOUS																									
Mfg. Site Transfer	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	B	●	●	●		●				
Material Suppliers	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	B	●	●	●		●				
New/Modified Mfg. Equipment		●		●			●	a			●			●	●	B									

a = termination equipment only

B = comparative data (unchanged vs. Changed) required

TABLE 14 - TABLE OF METHODS REFERENCED POLYMERIC RESETTABLE FUSES			
Stress	**NO.**	**Reference**	**Additional Requirements**
Pre- and Post-Stress Electrical Test	1	User Spec.	Test is performed except as specified in the applicable stress reference and the additional requirements in Table 14.
TEST NOT USED	2	----------	----------
TEST NOT USED	3	----------	----------
Temperature Cycling	4	JESD22 Method JA-104	1000 Cycles (-40°C to 125°C) Note: if 85°C part, 1000 Cycles will be at that temperature rating. Tri-temperature Pre and post stress required. Post-stress measurements to start 1 to 24 hours after test conclusion.
TEST NOT USED	5	----------	----------
Moisture Resistance	6	MIL-STD-202 Method 106	t = 24 hours/cycle. Note: Steps 7a & 7b not required. Unpowered test. Post-stress measurements to start 1 to 24 hours after test conclusion.
Biased Humidity	7	MIL-STD-202 Method 103	1000 hours 85°C/85% RH. Biased at10% of rated hold current Post-stress measurements to start 1 to 24 hours after test conclusion.
Operational Life	8	AEC-Q200-004	1000 hours (at 125°C) Note: if 85°C part, test temperature will be at that temperature rating. Post-stress measurements to start 1 to 24 hours after test conclusion.
External Visual	9	MIL-STD-883 Method 2009	Inspect device construction, marking and workmanship. Electrical test not required.
Physical Dimension	10	JESD22 Method JB-100	Verify the physical dimensions to the applicable user spec. Electrical test not required
Terminal Strength (Leaded)	11	AEC-Q200-004	Test leaded device lead integrity only
Resistance to Solvents	12	MIL-STD-202 Method 215	Note: Add Aqueous wash chemical - OKEM Clean or equivalent. Do not use banned solvents. Verify marking permanency. Not required for laser etched parts.
Mechanical Shock	13	MIL-STD-202 Method 213	Figure 1 of Method 213 SMD: Condition F LEADED: Condition C
Vibration	14	MIL-STD-202 Method 204	5g's for 20 minutes, 12 cycles each of 3 orientations. Test from 10-2000 Hz. Note: Use 8"X5" PCB .03 " thick. 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" of any secure points.

TABLE 14 - TABLE OF METHODS REFERENCED POLYMERIC RESETTABLE FUSES			
Stress	**NO.**	**Reference**	**Additional Requirements**
Resistance to Soldering Heat	15	MIL-STD-202 Method 210	Revised per latest Mil Spec. Cooling time prior to final measurement: 24 hrs. minimum
Thermal Shock	16	MIL-STD-202 Method 107	300 cycles (-40°C to 125°C) Note: if 85°C part, 300 Cycles will be at that temperature rating. Note: Maximum transfer time: 20 seconds, Dwell time-15 minutes. Medium: Air-Air Tri-temperature Pre and post stress required. Post-stress measurements to start 1 to 24 hours after test conclusion.
ESD	17	AEC-Q200-002	
Solderability	18	J-STD-002	For both Leaded & SMD. Electrical test not required. Magnification 50 X. Conditions: Leaded : Method A @ 235°C, Category 3 SMD: a) Method B, 4 hrs @ 155°C dry heat @ 235°C b) Method B @ 215°C, category 3 c) Method D Category 3 @ 260°C
Electrical Characterization	19	User Spec.	Parametrically test per lot and sample size requirements, summary to show Min, Max, Mean and Standard deviation at room as well as Min and Max operating temperatures.
Flammability	20	UL-94	V0 or V1 acceptable. Electrical test not required.
Board Flex (surface mount only)	21	AEC-Q200-005	Appendix 2 Note: 2mm Min.
Terminal Strength (SMD)	22	AEC-Q200-006	Appendix 1 Note: Force of 1.8kg for 60 seconds.
Short Circuit Fault Current Durability	31	AEC-Q200-004	
Fault Current Durability	32	AEC-Q200-004	
End-of-life Mode verification	33	AEC-Q200-004	
Jump Start Endurance	34	AEC-Q200-004	
Load Dump Endurance	35	AEC-Q200-004	

Note: Pre stress electrical tests also serve as electrical characterization if required data per Stress 19 is collected at that time.

TABLE 14A – Polymeric Resettable Fuses Process Change Qualification Guidelines for the Selection of Tests

4. Temperature Cycling
6. Moisture Resistance
7. Biased Humidity
8. Operation Life
9. External Visual
10. Physical Dimension (10 Samples only)
11. Terminal Strength (Leaded)
12. Resistance to Solvents
13. Mechanical Shock
14. Vibration
15. Resistance to Soldering Heat
16. Thermal Shock
17. ESD
18. Solderability
19. Electrical Characterization
20. Flammability
21. Board Flex (Surface Mount Only)
22. Terminal Strength (Surface Mount Only)
31. Short Circuit Current Durability
32. Fault Current Durability
33. End-of-Life Mode Verification
34. Jump Start Endurance
35. Load Dump Endurance

Note: A letter or "● " indicates that performance of that stress test should be considered for the appropriate process change.

Test # From Table 14	4	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	31	32	33	34	35	
MATERIAL																								
PTC Core Material			●	●	●						●	●			B					●	●			
Marking					●			●																
Terminal/Lead					●	●	●		●	●				●			●	●						
Terminal/Lead Attachment					●	●			●	●		●		●			●	●						
Protective Coating			●	●	●	●						●				●								
PROCESS																								
PTC Forming			●	●							●					●	●							
Substrate Singulation					●	●																		
Terminal/Lead Attachment			●	●	●		●					●		●			●	●						
Protective Coating			●	●	●	●						●												
Marking					●			1																
DESIGN																								
Form Factor					●	●									B									
Teminal Configuration (Kink)					●	●	●		●	●														
Characteristics Specification															B									
MISCELLANEOUS																								
Mfg. Site Transfer	●	●	●	●	●	●	●	1	●	●	●	●	●	●	B		●	●	●	●	●	●	●	

Note 1: For parts marked with ink only. Laser and stamped marked parts shall be exempt from this test.
Note 2: Test numbers are the last sub paragraph numbers of requirements or procedure paragraphs.
B = comparative data (unchanged vs. Changed) required

GLOSSARY OF TERMS/ABBREVIATIONS

1.	AEC	AUTOMOTIVE ELECTRONIC COUNCIL
2.	ESD	ELECTROSTATIC DISCHARGE
3.	FIT	FAILURE IN TIME
4.	DWV	DIELECTRIC WITHSTANDING VOLTAGE
5.	8D	DISCIPLINED APPROACH FOR PROBLEM SOLVING PROCESS

APPENDIX 1 - Definition of a Qualification Family

The qualification of a particular process will be defined within, but not limited to, the categories listed below. The supplier will provide a complete description of each process, case size and material of significance. There must be valid and obvious links between the data and the subject of qualification.

For devices to be categorized in a qualification family, they all must share the same major process and materials elements as defined below. All devices using the same process and materials are to be categorized in the same qualification family for that process and are qualified by association when one family member successfully completes qualification with the exception of the device specific requirements of section 4.2.

Prior qualification data 2 years old or newer obtained from a device in a specific family may be extended to the qualification of subsequent devices in that family provided the supplier can insure no process changes have been made.

For broad changes that involve multiple attributes (e.g. site, material(s), process(es)), refer to section 2.3, which allows for the selection of worst-case test vehicles to cover all the possible permutations.

1. Sub Assembly

Each process technology must be considered and qualified separately. No matter how similar, processes from one fundamental technology cannot be used for the other.

Family Requalification with the appropriate tests is required when the process or a material is changed. The important attributes defining a qualification family are listed below:

1) CAPACITOR TECHNOLOGY
* Aluminum Electrolytic
* Tantalum
* Ceramic
* Film
* Networks
* Trimmers

2) RESISTOR TECHNOLOGY
* Thin Film
* Thick Film
* Networks
*Trimmers
* Wirewounds
* Molded Metal Strip

3) INDUCTORS
* Fixed (Axial/Radial/SMD)
* Ferrite Cores
* Wirewound
* Multilayer
* Variable

4) TRANSFORMERS
* Pulse Transformers
* SMD (for DC TO DC CONVERTERS)
* Switch Mode Power Transformers
* SMD (for Pulse Applications)

5) VARISTORS
* Ring Varistors (Barium-Titanium Oxide)
* Disc Varistors (Zinc Oxide)
* Multilayer Surface Mounted Varistors

6) THERMISTORS
* For Motor Starting
* For Overcurrent Limiting
* For Temperature Compensation

7) CRYSTALS
* Metal AT CUT
* Metal AT STRIP
* Molded Surface Mounted
* Tuning Fork

8) RESONATORS
* Ceramic
* SAW resonators

2. Assembly Process

The processes for each package type must be considered and qualified separately. For devices to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family Requalification with the appropriate tests are required when the process or a material is changed. The supplier must submit technical justification to the user to support the acceptance of generic data with package type if different than the device to be qualified.

The important attributes defining a qualification family are listed below:

1) Package Type (e.g., 0402-0603-0805-1206 etc. - Ceramic caps)
(e.g., A-B-C-D-X size etc. - Tantalum caps)
(e.g., 1812-1210-1206-1008-0805 etc. - SMD Inductors)
(e.g., 0603-1206-1210-1825 etc. - SMD Resistors)

2) Assembly Site

3. Qualification of Multiple Families and Sites

When the specific product or process attribute to be qualified or requalified will affect more than a family, the qualification test vehicles should be three lots of a single device type from each of the technology and package families that are projected to be most sensitive to the changed attribute with sample sizes split to include a minimum of 30 pieces from each of 3 assembly lots from each assembly site.

Below is the recommended process for qualifying changes across many process and product families:

1) Identify all products affected by the proposed process changes.

2) Identify the critical structures and interfaces potentially affected by the proposed change.

3) Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces.

4) Define the product groupings or families based upon similar characteristics as they relate to the technology process and package families and device sensitivities to be evaluated, and provide technical justification for these groupings.

5) Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products, which will address each of the potential failure mechanisms and associated failure modes.

6) Robust process capability must be demonstrated at each site (e.g. control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process step(s).

APPENDIX 2 - Certificate of Design, Construction and Qualification (CDCQ)

The following information, as applicable, is required to identify a component, which has met the requirements of this specification. This page is available as a stand-alone document.

Supplier		Lead/terminal attachment method	
User P/N(s)		Package outline drawing	
Supplier P/N(s)		Flammability rating	
Data sheet		ESD characterization(s)	
Assembly Location		Lead/Termination material	
Process Identifier		Lead plating/coating	
Final QC Facility Location		Construction cross section	
Family number		Package Subcontractor(s)	
Technology description		Element composition	
All dimensions in millimeters		Solvent exposure restriction	
Metallization material		Marking method	
Number of active layers		Exceptions taken to AEC- Q200	
Electrode/Internal element attachment method		Subassembly location	
Thickness range		Insulation material	
Package material			

Attachments:
1) Cross section photo.
2) Package outline drawing.
3) Special test circuits.
4) Letter stating exceptions taken to AEC-Q200.

Requirements:
1) A separate CDCQ shall be submitted for each family as defined by Appendix 1 and Appendix 2

2) Document shall be signed by a responsible individual at the supplier who can verify that all of the above information is correct.

Type name and sign.

Completed by:	Date:	Certified By:	Title	Date:

APPENDIX 3 - Qualification Test Plan Format

The supplier is requested to complete and submit the Passive Component Qualification Plan as part of the pre-launch Control Plan whenever production approval submission is required. Acceptance and subsequent sign-off of the plan will establish a qualification agreement between the user and the supplier determining requirements for both new parts and process changes prior to commencement of testing. Where “family” data is being proposed, the plan will document how the reliability testing previously completed fulfills the requirements outlined in this specification. An approved copy of the qualification plan should be included with each production approval submission.

The test plan section of the form should detail ONLY the testing that will be performed on the specific part shown. **Testing MUST include the additional requirements listed in the applicable table 2-14.** For process change qualifications, multiple parts can be included on the same plan. Supporting generic or family data reports should be noted in the comment section and attached. When requesting use of generic or family data, attach a separate page detailing similarities or differences between parts referencing the criteria in Appendix1. There must be valid and obvious links between the data and the subject of qualification.

The example below is provided to demonstrate how the Qualification Plan Form should be used. In this case, a ceramic multilayer capacitor was chosen as being representative of a typical new part qualification requesting reduced component testing by including generic test data. The part comes from a supplier who previously qualified the package, assembly site etc. This ***EXAMPLE*** is shown for illustration purposes only and should not limit any requirements from Table 1 – 14 herein.

Automotive Electronics Council
Component Technical Committee

EXAMPLE Passive Component Qualification Test Plan

Rev: - 2/3/96

User P/N : N611045BFDDAARA

User Component Engineer : John Doe

User Spec. # : ES-N6110450FDAARA

General Specification : AEC-Q200

Supplier : Sam's Discount Capacitor

Supplier Manufacturing Site : Shanghai, China

Supplier P/N: N611045BFDDAARA

Required production approval Submission Date : 5/1/96

Family Type : X7R1206 Ceramic

Reason for Qualification : New device Qualification

Item	Test	Test conditions	Exceptions	Est. Start	Est. Comp.	# Lots	S. S.	Additional Requirements
1	Electrical Test	@ -55°C, 25°C, 125 °C		4/1/96	4/5/96	all	all	
3	High Temp Exposure	1000 Hours @ 150°C		4/11/96	6/24/96	3	40	
4	Temperature Cycling	1000 cycles (-55°C to +125°C)		4/15/96	6/24/96			
5	Destructive Physical Analysis			4/22/96	4/29/96			
6	Moisture Resistance	Cycled 25°C to 65°C, 80-100% RH, 24 hours/cycle 10 Cycles		4/29/96	5/27/96			
7	Biased Humidity	1000 hours 85°C/85RH	Use attached generic data for this package related test. Comment #1	4/28/96	6/24/96			generic data uses +70C/85% (rather than 85C) Rated and 1.3V. Add 100K Ohm resistor.
8	Operating Life	1000 hours 125°C with Full rated Voltage		4/15/96	6/24/96			
9	External Visual	Per Spec.		4/22/96	4/29/96			
10	Physical Dimensions	Per user(s) Spec.		4/22/96	4/28/96			
12	Resistance to Solvents	MIL STD 215 and Aqueous Wash materials		4/22/96	4/26/96			
13	Mechanical Shock	½ Sine Pulse 1500g Peak		5/19/96	5/26/96			

Test summaries are to include mean, std. Deviation, min. & max. Reading for all endpoint tests.

Comments:

1. Supplier requests 1 lot qualification of this device type in addition to attached reliability reports of similar parts.

Prepared by:
(supplier)

Approved by:
(User Engineer)

Example of Passive Component Qualification Plan

APPENDIX 4 - Data Presentation Format and Content

The supplier is required to complete and submit an Environmental Test Summary and Parametric Verification Summary with each Passive Component production approval submittal. Figure 4-1 is an ***EXAMPLE*** of a completed Environmental Test Summary. The format shall be followed.

Production Part Approval - Environmental Test Summary

EXAMPLE

SUPPLIER Sam's Discount Capacitors		USER PART NUMBER N611045BFDAARA			
NAME OF LABORATORY SDS Qual Lab.		PART NAME Ceramic Capacitor			
Test #	Description	Test Conditions	# Lots Tested	Qty Tested	Number Failed
3	High Temp. Exposure	Per Spec.	3	120	0
5	Destructive Physical Analysis	Per Spec.	3	15	0
9	External Visual	Per Spec.	3	260	0
10	Physical Dimensions	Per Spec.	3	30	0
12	Resistance to Solvents	Per Spec.	1	5	0
13	Mechanical Shock	½ Sine Pulse 1500g	3	90	0

Figure 4-1 Environmental Test Summary

Figure 4-2 is an ***EXAMPLE*** of a completed Parametric Verification Summary. The format shall be followed.

Production Part Approval - Parametric Verification Summary

Supplier SAM's Discount Passive Components			Part Number N611045BFDAARA				
Lot Number 394A			Temperature -55°C				
Test Name	User Spec. LSL	User Spec. USL	Min.	Max.	Mean	Std. Dev.	Cpk
Capacitance	0.09 µF	0.11 µF	0.0971 µF	0.1086 µF	0.103 µF	0.0013 µF	1.79
DF	------	±2.5%	1.07%	1.98%	1.6%	.092%	3.79
IR	20GΩ	------	40GΩ	100GΩ	70GΩ	30GΩ	7.03
Temperature Coefficient	-15.0%	+15%	-14.83%	-5.97%	-11.4%	1.01%	1.19

Figure 4-2 Parametric Verification Summary

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
-	April 30, 1996	Initial Release.
A	June 16, 1997	(1.1.1) Add Crystals, Resonators, Ferrites (2.1) Changed "qualification program" to "document" Added "user's" to item #2. (2.3) Changed 2-10, 2A-10A to 2-13,2A-13A (2.4.5) Changed 2-10 to 2-13 (2.6) " " (2.7) " " (3.1) " " (3.2.2) Changed 2-10, 2A-10A to 2-13,2A-13A (4.1) Table 1 - Remove N on Test 12. Add S on Test 21-22 Table 2 - Remove Test 24 Add 1.5mm to Test 15 Table 2A - Remove Test 24 Table 4 - Changed temperature on Test 16 Table 9 - Added 230C, term. coverage Test 15 Changed minutes to seconds Test 16 Tables 2-10- Added 24 Hour meas. Tests3,4,6-8. Add 10-2000 Hz on Test 14 Tables 11-13-Added Tables 11-13, 11A-13A Appendix 2 - Added resp. Individual to requirement 2
B	March 15, 2000	Removed CDF designation through document. Removed Chrysler, Delco, and Ford logo from each heading. Removed Automotive Grade through document. Added Component Technical Committee to each heading. (1.2.3) Replaced Automotive with AEC Tables 14 –14A Added Tables for Polymetric Resettable Fuses. Changed all references to Tables 2– 13 to 2–14 Changed all references to Tables 2A – 13A to 2A –14A (4.1) Changed reference to Table 1-13 to 1-14 (2.4.1) Changes to lot requirements are designated in Table1 herein Tables 2-13, item 18 – Reversed Method a and b for SMD solderability requirements Table 3, item 16 – Changed dwell time to 15 minutes Table 5, item 16 – Changed dwell time to 15 minutes Table 6, item 21 – Added 3mm board flex for COG devices Table 1, Added Note A and Note B. Table 1, item 18 - Changed sample size from 10 to 15. Table 1, item 18 – Added each condition. Legend for Table 1- Added Note A and B
C	June 16, 2005	Acknowledgements – latest information on members Table of Contents – page number corrections (1.1.1) Temperature Grades – definition of AEC qualified (1.2.1) MIL-PRF-27 reference correction (1.2.3) Addition of AEC subspec test method references (2.3) editorial

(2.4.3) editorial
(3.2) Added section: Qualification of a Lead (Pb) – Free Device
(3.3.2) comparative testing of parts
(4.3) Added section: Lead (Pb) – Free Specific Tests
(4.4) Data maintenance per TS-16949
Table 1: Solderability note C and legend description
Test 21: AEC-Q200-005 reference in Table of Tests
Test 22: AEC-Q200-006 reference in Table of Tests
Test 19: B reference in Change tables and legend description
Test 27: AEC-Q200-007 reference in Table of Tests
Test 8: MIL-PRF-27 reference in Table of Tests #5
Appendix 1, family 7 & 8

ATTACHMENT 1

AEC - Q200 - 001

FLAME RETARDANCE TEST

METHOD - 001

PASSIVE COMPONENT FLAME RETARDANCE TEST

1.0 SCOPE

1.1 DESCRIPTION:

The purpose of this specification is to assure a device will not flame due to self-heating when full automotive battery potential is applied. This test applies to all devices that, under normal operation, are not intended for use at full automotive battery potential.

1.2 Reference Documents:

Not Applicable

2.0 EQUIPMENT:

2.1 Test Apparatus:

The following items are required when performing this test:

a) A circuit board suitable for mounting test devices

b) A regulated, variable voltage power supply capable of maintaining 32VDC at a clamp current up to 500ADC.

c) A temperature sensing and recording system capable of continuous monitoring of temperatures to a maximum of 500C.

d) A visual method of monitoring flame duration.

3.0 TEST PROCEDURE:

3.1 Sample Size:

The total number of components and lots to be tested are listed in Table 1 of AEC-Q200 specification.

3.2 Test Environment :

Devices shall be mounted to the test board in their normal mounting configuration and subjected to voltages from 9.0 to 32.0 VDC (current clamped up to 500A) in 1.0 VDC increments. Each voltage level shall be applied for a minimum of one hour, or until the device is either electrically open or a failure described in Paragraph 4.0 occurs. The test board shall be horizontal, with the component on the underside if a leaded device and on the top side if a surface mounted device. The test shall be conducted at 22C $\pm$ 5C in still air. The temperature sensor shall be placed in contact with, but not adhered to, the outer surface of the device centered along its body for parts rated at one Watt and below, or at a distance of 1mm from the outer surface of the device body for devices rated above one Watt, as illustrated in Figure 1.

3.3 Measurement:

Prior to Flame Retardance testing, complete the electrical characterization (TST NO. 19) functional tests. The DC current shall be monitored continuously during the test to determine when the device is electrically open. The temperature sensing and recording system shall monitor temperature throughout the test.

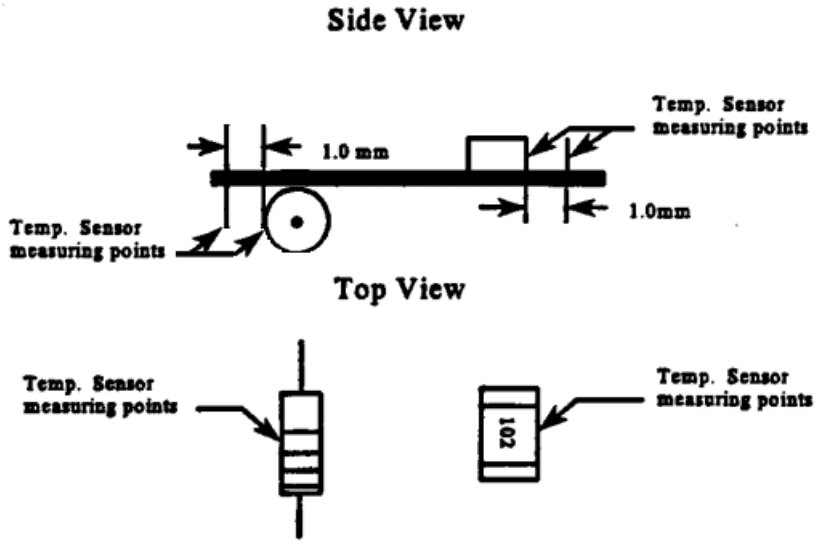


Figure 1 Leaded and Surface Mount Device Temperature Sensor contact points

4.0 FAILURE CRITERIA

The following constitutes a failure:

a) A flame over 3.0 seconds duration

b) An explosion

c) A temperature above 350C sustained for over 10 seconds

Any device that electrically opens or changes value outside part tolerance without causing any of the above shall not be considered a failure. Should a device open prior to attaining the maximum voltage or current described in 3.0, that device shall be replaced. The replaced device shall be subjected to 32 VDC current clamped up to 500 ADC and decreased in 1.0 VDC/hour increments until the voltage at which the first device opened is attained or until all parts are open, whichever occurs first. This assures that the part will meet specification requirements throughout the required test voltage range.

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
	April 30, 1996	Initial Release.
A	March 15, 2000	Removed CDF designation through document. Removed Chrysler, Delco, and Ford logo from each heading. Add Component Technical Committee to each heading. Figure 1 (Side View): Change leaded component and temperature sensor measuring point to the bottom side of the circuit board.

ATTACHMENT 2

AEC - Q200 - 002

HUMAN BODY ELECTROSTATIC DISCHARGE TEST

METHOD - 002

PASSIVE COMPONENT HUMAN BODY MODEL (HBM) ELECTROSTATIC DISCHARGE (ESD) TEST

1.0 SCOPE

1.1 Description:

The purpose of this specification is to establish a reliable and repeatable procedure for determining passive component HBM ESD sensitivity.

1.2 Reference Documents:

IEC 801-2 (1990)

1.3 Terms and Definitions:

The terms used in this specification are defined as follows.

1.3.1 Component Failure:

A condition in which a component does not meet all the requirements of the acceptance criteria, as specified in section 5 following the ESD test.

1.3.2 Device Under Test (DUT):

An electronic component being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD):

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.4 Electrostatic Discharge Sensitivity:

An ESD voltage level which causes component failure.

1.3.5 ESD Simulator:

An instrument that simulates the passive component human body model ESD pulse as defined in this specification.

1.3.6 Ground Plane:

A common electrical reference point for the DUT, ESD simulator, and auxiliary equipment.

1.3.7 Human Body Model (HBM):

A capacitance and resistance model that characterizes a person as a source of electrostatic charging for automotive conditions, as shown in Figure 1, and the resulting ESD pulse meeting the waveform criteria specified in this test method.

1.3.8 Maximum Withstanding Voltage:

The maximum ESD voltage at which, and below, the component is determined to pass the failure criteria requirements specified in section 4.

1.3.9 PUT:

PUT is the pin and/or terminal under test.

2.0 EQUIPMENT:

2.1 Test Apparatus:

The apparatus for this test consists of an ESD pulse simulator with an equivalent passive component HBM ESD circuit as shown in Figure 1. The simulator must be capable of supplying pulses that meet the waveform requirements of Table 1 and Figure 3 using the coaxial target specified in section 2.2.1.

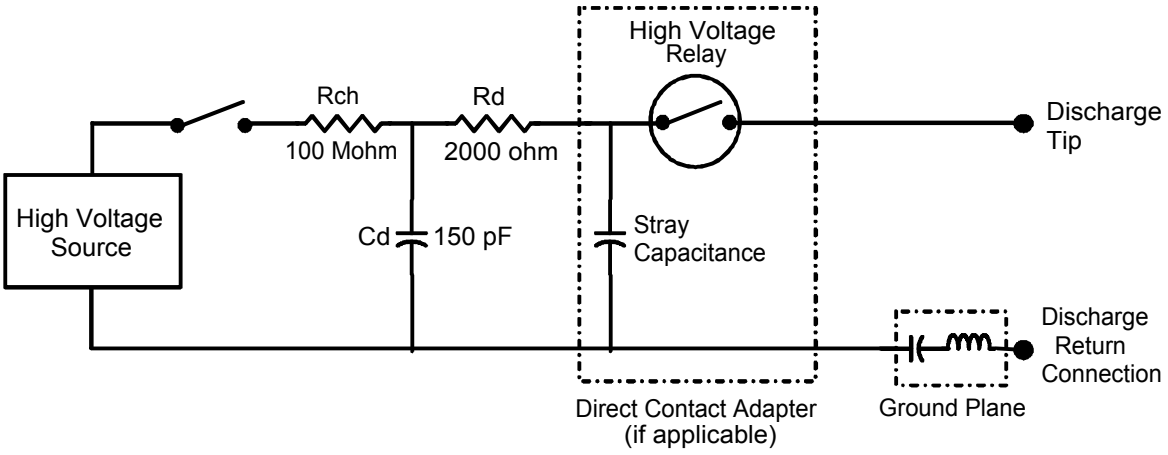


Figure 1: Equivalent Passive Component HBM ESD simulator circuit

2.2 Measurement Equipment:

Equipment used to verify conformance of the simulator discharge waveform to the requirements as specified in Table 1 and Figure 3 shall be either an analog oscilloscope with a minimum bandwidth of 1 GHz or a digital oscilloscope with a minimum sampling rate of 2 gigasamples per second and a minimum bandwidth of 1 GHz. Each instrument shall have a 50 ohm input impedance. A faster oscilloscope (larger bandwidth and/or higher sampling rate) may be required to fully characterize the ESD waveform.

2.2.1 Coaxial Target:

The coaxial target shall be a current-sensing transducer as specified by IEC 801-2 (1990), or equivalent. The target is used to verify the ESD simulator waveform as defined in sections 2.3, 2.3.1, and 2.3.2.

2.2.2 Ground Plane:

The ground plane is a common electrical reference point with dimensional requirements of a 1 mm minimum thickness and a 1 m^2 minimum area. The ground plane is connected to earth ground by a ground strap as short and as wide as possible; length ≤ 1 m, width ≥ 5 mm, and inductance ≤ 2 μH.

2.2.3 Probe:

The probe used to verify the ESD simulator charging voltage, as defined in sections 2.3.2 and 2.4, shall be an electrometer probe with an input impedance ≥ 100 Gigohm.

2.2.4 20 dB Wideband Attenuator:

A 20 dB wideband attenuator may be required depending on the vertical sensitivity of the oscilloscope. The attenuator shall be a 50 ohm, 20 dB wideband attenuator with a bandwidth of 20 GHz and 2 kW peak pulse power. When using the attenuator, it shall be attached to the output of the coaxial target during the ESD simulator qualification and waveform verification as defined in sections 2.3 and 2.4.

2.3 ESD Simulator Qualification:

ESD simulator calibration and qualification must be performed during initial acceptance testing and whenever the simulator is serviced. A period of six (6) months is the maximum permissible time between full qualification tests. The ESD simulator must meet the waveform parameter requirements for all voltage levels as defined in Table 1, section 2.3.1, and section 2.3.2. If at any time the waveforms do not meet the requirements of Table 1 and Figure 3, the testing shall be halted until waveforms are in compliance.

2.3.1 Simulator Qualification Setup:

a. The simulator qualification setup shall be configured according to the equivalent schematic shown in Figure 2. Note that a 20 dB wideband attenuator may be required as shown in Figure 2 depending on the vertical sensitivity of the oscilloscope.

b. The coaxial target shall be located on and bonded to the center of the ground plane. The target output shall be connected to the oscilloscope through a 50 ohm double-shielded, high frequency, semi-rigid cable with length ≤ 1 meter. The cable shall not be looped and shall be insulated from the ground plane.

c. The horizontal time base and vertical amplifier level of the oscilloscope shall be configured in order to view the rise time of the ESD waveform. The horizontal sweep shall be set to single event trigger.

d. The ESD simulator high voltage ground shall be directly connected to the ground plane by a grounding strap with length ≤ 1 meter and an inductance ≤ 2 μH. The ESD simulator shall be set up and operated according to its instruction manual.

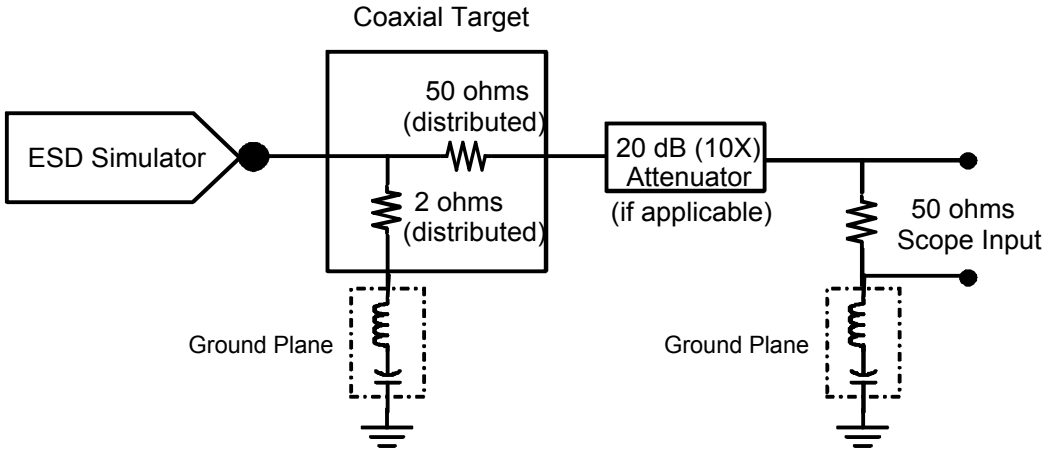


Figure 2: Equivalent schematic for Simulator Qualification

2.3.2 Simulator Qualification Procedure:

a. To calibrate the display voltage of the ESD simulator, adjust the simulator voltage to the desired level and polarity. With the electrometer in direct contact with the discharge tip (see Figure 1), verify the voltage setting at levels of ± 500 V, ± 1 kV, ± 2 kV, ± 4 kV, ± 8 kV, ± 12 kV, ± 16 kV, and ± 25 kV. The electrometer reading shall be within ± 10% for voltages from 200 V to ≤ 25 kV.

b. For Direct Contact Discharge Qualification, discharge to the coaxial target at each voltage level and polarity shown in Table 1. Record the rise time and first peak current values and verify the parameters meet the requirements of Table 1. Figure 3 illustrates a typical discharge waveform to a coaxial target. The simulator must meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at all voltage levels.

c. For Air Discharge qualification, the ESD simulator shall be placed a distance of ≥ 15 mm from the coaxial target sphere. The ESD simulator, with the air discharge probe attached, shall be held perpendicular (± 15°) to the target. From this position, the simulator air discharge probe shall be slowly (≤ 5 mm/second) moved towards the target until a single discharge occurs. Only single event discharge waveforms shall be acceptable. Test voltages for the air discharge are ± 12 kV, ± 16 kV, and ± 25 kV. Figure 3 illustrates a typical discharge waveform to a coaxial target. The slow approach method specified above minimizes multiple discharges, discharges at lower voltage levels, and ringing in the measurement equipment.

2.4 ESD Simulator Charge Verification:

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, ESD simulator charge verification shall be performed before each daily use. With the electrometer in direct contact with the discharge tip (see Figure 1), verify the voltage setting at levels of ± 500 V, ± 1 kV, ± 2 kV, ± 4 kV, ± 8 kV, ± 12 kV, ± 16 kV, and ± 25 kV. The electrometer reading shall be within ± 10% for voltages from 200 V to ≤ 25 kV. If at any time the simulator charge does not meet the requirements of Table 1, the testing shall be halted until the simulator is in compliance and all ESD testing performed since the last passing charge verification shall be considered invalid.

Table 1: Direct Contact and Air Discharge ESD waveform parameter requirements

ESD Discharge Method	Indicated Voltage (kV)	First Peak Current, Ip (A)	Rise Time, tr (ns)
Direct Contact Discharge	0.5 ± 0.05	1.87 +0.60/-0	0.7 to 1.0
	1.0 ± 0.1	3.75 +1.12/-0	0.7 to 1.0
	2.0 ± 0.5	7.50 +2.25/-0	0.7 to 1.0
	4.0 ± 0.5	15.0 +4.50/-0	0.7 to 1.0
	8.0 ± 0.8	30.0 +9.0/-0	0.7 to 1.0
Air Discharge	25.0 ± 2.5	Not Specified	Not Specified

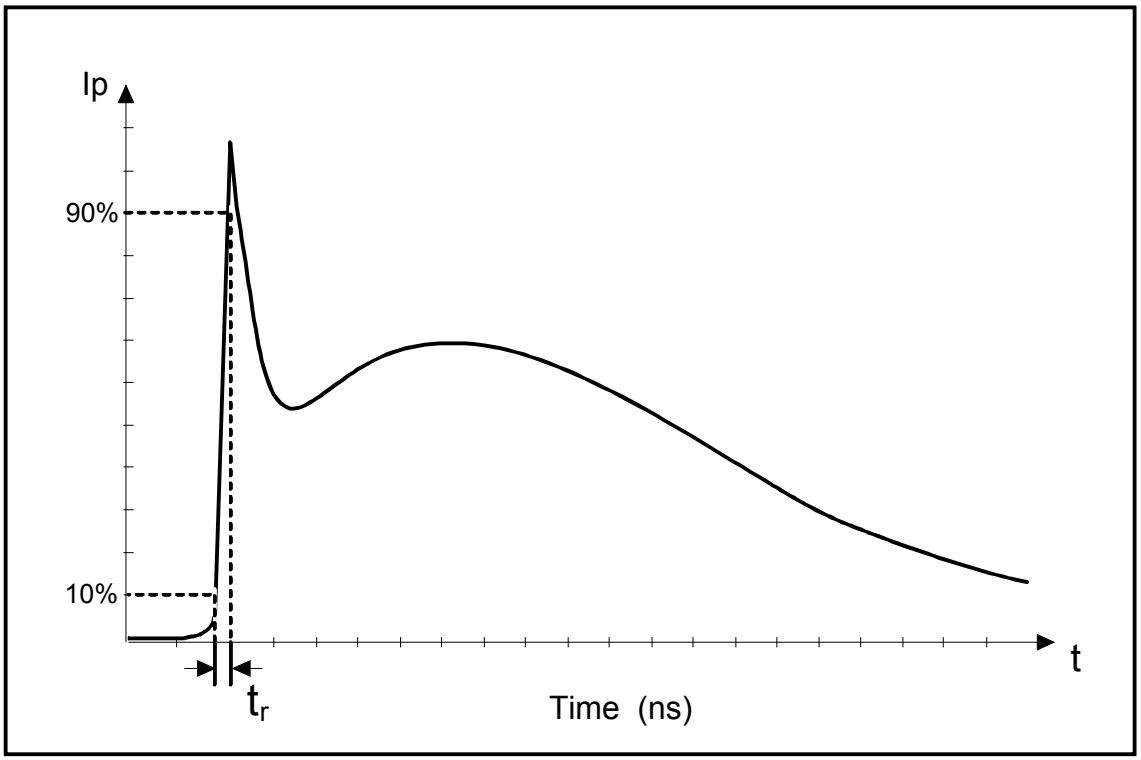


Figure 3: Typical Direct Contact and Air Discharge *PASSIVE COMPONENT* HBM ESD discharge waveform to a coaxial target

3.0 TEST PROCEDURE:

3.1 Sample Size:

Each sample group shall be composed of 15 components, as specified in Table 1 of AEC - Q200. Each sample group shall be stressed at one (1) voltage level using all pin and/or terminal combinations specified in section 3.2. The use of a new sample group for each stress voltage level is recommended. It is permitted to use the same sample group for the next stress level if all components in the sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level.

3.2 Pin and/or Terminal Combinations:

Each pair of pins and/or terminals and all combinations of pin and/or terminal pairs for each component shall be subjected to one (1) pulse at each stress voltage polarity following the ESD levels stated in Figure 4. Any pin and/or terminal not under test shall be in an electrically open (floating) state. A sufficient number of ESD levels must be tested to either: a) demonstrate the component can pass a 25 kV Air Discharge exposure, or b) determine the pass/fail transition region between two (2) consecutive ESD test levels. If an expected failure level cannot be estimated, the test flow diagram of Figure 4 may be used to minimize the amount of testing required.

3.3 Test Environment:

Each component shall be subjected to ESD pulses at 22C ± 5C. For all Air Discharge testing, the relative humidity shall be 30% to 60%.

3.4 Measurements:

Prior to ESD testing, complete parametric testing (initial electrical verification) shall be performed on all sample groups and all components in each sample group per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification. If using an allowable parametric shift as a failure criterion, a data log of each component shall be made listing the applicable parameter measurement values. The data log will be compared to the parameters measured during final electrical test verification testing to determine the failure criteria of section 4.

3.5 Test Setup:

a. Ensure that the daily ESD simulator charge verification procedure (section 2.4) has been performed before applying discharges to the DUT.

b. The ESD simulator high voltage ground shall be directly connected to the ground plane by a grounding strap with a length ≤ 1 meter and an inductance ≤ 2 μH.

c. All DUTs are considered sensitive to ESD until proven otherwise and shall be handled accordingly (reference internal procedures for proper handling of ESD sensitive components).

d. The DUT must pass complete parametric testing (initial electrical verification) as defined in section 3.4 prior to any application of ESD stress voltage levels.

3.6 Detailed Procedure:

3.6.1 Direct Contact Discharge:

a. The ESD simulator shall be placed in direct contact with each PUT specified in section 3.2.

b. Each PUT within a sample group shall be tested at a stress voltage level specified in the test flow diagram of Figure 4 using the Direct Contact discharge probe. Two (2) discharges shall be applied to each PUT within a sample group and at each stress voltage level, one (1) with a positive polarity and one (1) with a negative polarity.

c. After each discharge to the PUT, residual charge remaining on the DUT shall be dissipated by briefly connecting a one (1) megohm resistor between the PUT discharge location and/or ground point of the DUT and the ground of the test setup.

d. Repeat the procedure for all components within the sample group.

e. Using the next sample group, select another direct contact stress voltage level and repeat the above procedure until all sample groups have been tested at a specified voltage level. It is permitted to use the same sample group for the next stress voltage level if all components in the sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level.

f. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the acceptance criteria requirements specified in section 5. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

3.6.2 Air Discharge:

a. Using a new sample group, each PUT specified in section 3.2 shall be tested at an air discharge stress voltage level specified in the test flow diagram of Figure 4 using the Air Discharge probe. It is permitted to use the same sample group for the next stress voltage level if all components in the sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level.

b. The ESD simulator shall be placed ≥ 15 mm away from the PUT. The simulator, with the Air Discharge probe, shall be held perpendicular to the PUT discharge location. The probe shall be slowly moved towards the PUT (e.g., ≤ 5 mm/second) until a single discharge is obtained.

c. If no discharge occurs, continue moving the probe towards the DUT until the simulator discharge probe contacts the PUT discharge location. If the simulator makes contact with the PUT discharge location and discharge occurs, discontinue testing at the stress voltage level and location. A test board with closely spaced lead wires or metal runners may prevent discharging to an intended PUT and result in an arcing phenomenon. When this situation occurs, multiple test boards with a reduced number of lead wires or metal runners shall be used.

d. Two (2) discharges shall be applied to each PUT within a sample group at the air discharge stress voltage level, one (1) with a positive polarity and one (1) with a negative polarity.

e. After each discharge to the PUT, residual charge remaining on the DUT shall be dissipated by briefly connecting a one (1) megohm resistor between the PUT discharge location and/or ground point of the DUT and the ground of the test setup.

f. Repeat the procedure for all components within the sample group.

g. Using the next sample group, select another air discharge stress voltage level and repeat the above procedure until all sample groups have been tested at a specific voltage level. It is permitted to use the same sample group for the next stress voltage level if all components in the sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level.

h. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the acceptance criteria requirements specified in section 5. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

4.0 FAILURE CRITERIA

A component will be defined as a failure if, after exposure to ESD pulses, the component fails any of the following criteria:

1. The component exceeds the allowable shift value. Specific parameters and allowable shift values shall be defined in the applicable user device specification. During initial parametric testing, a data log shall be made for each component listing the applicable parameter measurement values. The data log will be compared to the parameters measured during final parametric testing to determine the shift value. Components exceeding the allowable shift value will be defined as a failure.

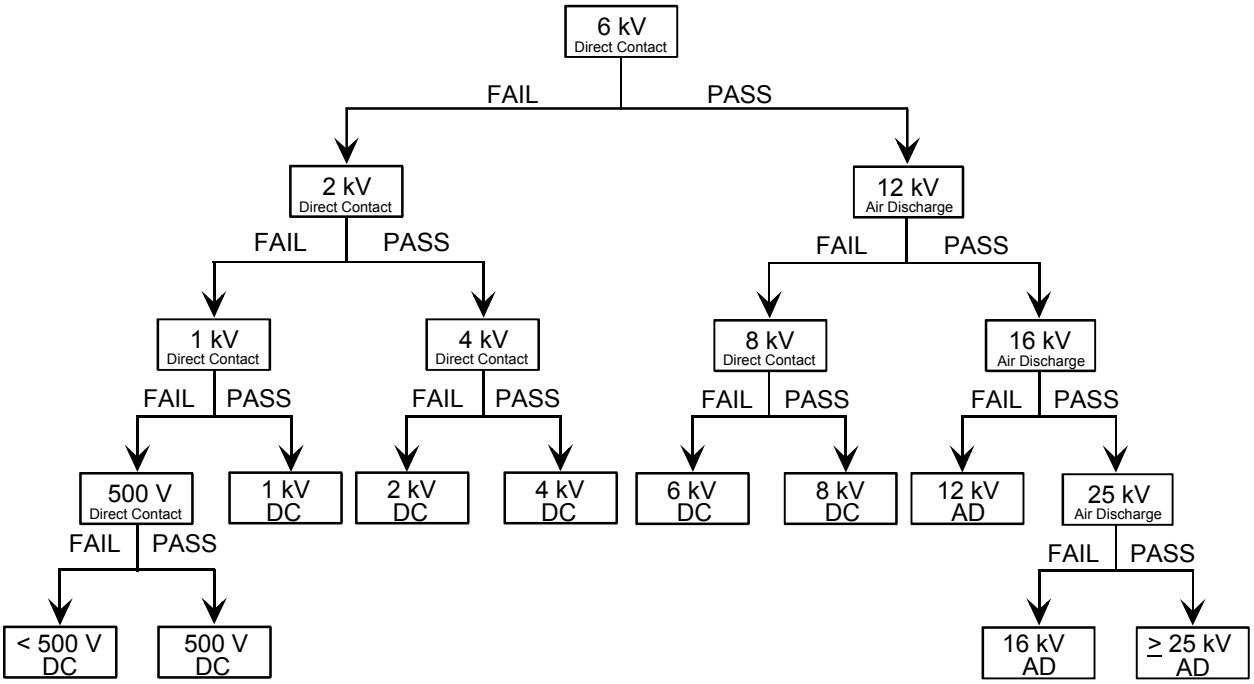
2. The component no longer meets the user device specification requirements. Complete parametric testing (initial and final electrical verification) shall be performed per applicable user device specification.

5.0 ACCEPTANCE CRITERIA:

A component passes a voltage level if all components stressed at that voltage level pass. All the samples used must meet the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 2, classify the components according to the highest ESD voltage level survived during ESD testing. The supplier shall define the ESD withstanding voltage for each component.

Table 2: Passive Component HBM ESD classification levels
(DC = Direct Contact Discharge, AD = Air Discharge)

Component Classification	Maximum Withstand Voltage
1A	< 500 V (DC)
1B	500 V (DC) to < 1000 V (DC)
1C	1000 V (DC) to < 2000 V (DC)
2	2000 V (DC) to < 4000 V (DC)
3	4000 V (DC) to < 6000 V (DC)
4	6000 V (DC) to < 8000 V (DC)
5A	8000 V (DC) to < 12,000 V (AD)
5B	12,000 V (AD) to < 16,000 V (AD)
5C	16,000 V (AD) to < 25,000 V (AD)
6	≥ 25,000 V (AD)



Note 1: Classify the components according to the highest ESD voltage level survived during ESD testing.

Figure 4: Passive Component HBM ESD test flow diagram
(DC = Direct Contact Discharge, AD = Air Discharge)

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
	April 30, 1996	Initial Release.
A	March 15, 2000	Removed CDF designation through document. Removed Chrysler, Delco, and Ford logo from each heading. Add Component Technical Committee to each heading.

ATTACHMENT 3

AEC - Q200 - 003

BEAM LOAD (BREAK STRENGTH) TEST

METHOD - 003

PASSIVE COMPONENT
SURFACE MOUNTED CERAMIC CAPACITORS
BEAM LOAD (BREAK STRENGTH) TEST

1.0 SCOPE

1.1 DESCRIPTION:

This specification establishes the procedure and criteria for evaluating break strength.

1.2 Reference Documents:

Not Applicable

2.0 EQUIPMENT:

2.1 Test Apparatus:

The apparatus required for testing shall be equivalent to the fixture shown in Figure 1.

3.0 TEST PROCEDURE:

3.1 Sample Size:

The total number of components and lots to be tested are listed in Table 1 of AEC-Q200 specification.

3.2 Test Environment :

Place the part in the beam load fixture. Apply a force until the part breaks or the minimum acceptable force level required in the user specification(s) is attained.

3.3 Measurement:

Prior to beam load testing, complete the external visual (TST NO. 9) test. Record the force level at which the part breaks to conclude the test.

Breaking strength
Tested with the fixture described below

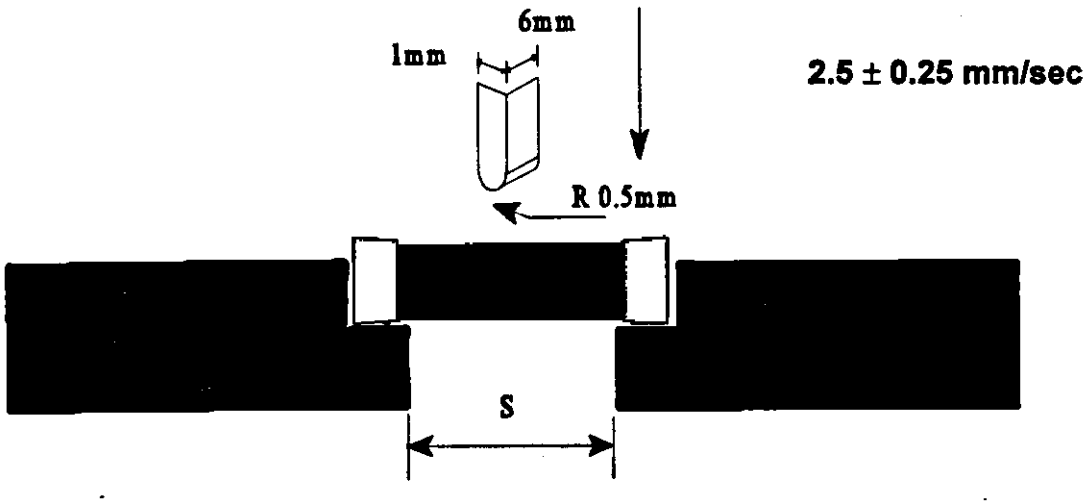


Figure 1: Typical equivalent circuit for Beam Load Test
Note: S = .55 ± 0.05 of the nominal length of Device Under Test

4.0 FAILURE CRITERIA

During (if applicable) and after subjection to test, part rupture prior to any minimum user force requirement shall be considered a failure.

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
	April 30, 1996	Initial Release.
A	March 15, 2000	Removed CDF designation through document. Removed Chrysler, Delco, and Ford logo from each heading. Add Component Technical Committee to each heading.

ATTACHMENT 4

AEC - Q200 - 004

MEASUREMENT PROCEDURES FOR RESETTABLE FUSES

METHOD 004

PASSIVE COMPONENT
MEASUREMENT METHODS FOR
RESETTABLE FUSES

1.0 SCOPE

1.1 **Description:**

This method covers the test and measurement methods for resettable fuses based on polymeric materials with positive temperature coefficient of resistance. The purpose of this specification is to provide users of such components means to compare polymeric positive temperature coefficient (PPTC) based resettable fuses against an established standard performance requirements tested in accordance with an established test method. This method provides supplemental information required to perform tests described in Table 14 of AEC-Q200.

1.2 **Terms and Definitions**:

1.2.1 Absolute Maximum Resistance, A_{max}: Maximum functional resistance of devices before and after stress tests.

1.2.2. Absolute Minimum Resistance, R_{amin}: Minimum functional resistance of devices before and after stress tests.

1.2.3 Core Material (Chip): A singulated sub-component of resettable fuse material that contains conductive polymer and two electrodes that may be coated with solder.

1.2.4 Electrical Current Type: Unless otherwise specified, direct current power source shall be used.

1.2.5 Lot: Unless otherwise specified, a lot shall consist of devices manufactured to the same part drawing number, assembled at the same location using the same production techniques, materials, controls and design.

1.2.6 Maximum Hold Current, I_{hold}: The maximum current that any device of a given product designation (part number) is guaranteed to hold without tripping, at specified temperature conditions, and under specified circuit and/or source conditions.

1.2.7 Maximum Hold Current at Temperature, $I_{hold@T}$: *Maximum hold current* at the specified ambient temperature as specified in *User Specification.*

1.2.8 Maximum Operating Voltage, V_{max}: The maximum voltage a resettable fuse is designed to tolerate as specified on device User Specifications.

1.2.9 Maximum Resistance, R_{max}: The maximum resistance of a device that has not been tripped in as-shipped condition and measured at room temperature.

1.2.10 Maximum Short Circuit Current, I_{scmax}: The maximum current used to perform short circuit current durability test based on device operating parameters specified on the user specification.

1.2.11 Minimum Resistance, R_{min}: The lowest specified resistance of a device that has not been tripped in as-shipped condition and measured at *room temperature*.

1.2.12 Room Temperature: Unless otherwise defined, the temperature range of 25±5ºC is defined as the room temperature.

1.2.13 Passive Resistance: Resistance of a device measured with no power (excluding measurement instrument supplied power) applied to the device.

1.2.14 Steady State: A change of less than 1% in the *power dissipation* over a one minute period.

1.2.15 Still Air Environment (Non-forced Air Environment): An environment where the only air movement is from natural convection due to heating or cooling of ambient air.

1.2.16 Time-to-Trip, TtT: Time-to-trip is defined as an elapsed time from the application of a specific amount of current to a device-under-test at a specific ambient temperature specified in the user specification to the point where the device-under-test reaches the *tripped state*.

1.2.17 Trip Current, I_{trip}: The minimum current guaranteed to trip any device of a given product designation in a specified time, at specified temperature conditions, and under specified circuit and/or source conditions.

1.2.18 Tripped Power Dissipation, P_d: Power dissipation is the product of the current flowing through a device in the *tripped state* and the voltage across the device.

1.2.19 Tripped State: A device is in the tripped state when the voltage across the device-under-test rises to 80% of the open circuit source voltage, or the resistance of the device increases by a factor of 40 times or more of the maximum specified resistance at the test environment temperature.

2.0 TEST CONDITION REQUIREMENTS

2.1 Device Mounting:

2.1.1 Mounting of Device for Electrical Test:

2.1.1.1 Leaded: Where applicable and unless otherwise specified, devices shall be mounted for electrical testing to the test apparatus via a pair of spring loaded clips. Leaded devices with formed leads shall be clipped within 5 mm from the base of the form away from the device body. Leaded devices with non-formed leads shall be clipped at 5 to 10 mm from the bottom of the body of the part.

2.1.1.2 SMD: Where applicable and unless otherwise specified, devices shall be mounted for electrical testing on printed circuit boards where the power dissipation of the mounted device is consistent with the typical power dissipation value found in User Specification. Devices shall be reflowed on to test boards using a reflow oven, or equivalent, and an appropriate reflow temperature-time profile. Devices shall be left at room temperature for a minimum of 24 hours prior to starting pre-stress tests.

2.2 Test Power Source: Unless otherwise specified, the standard open circuit test voltage shall be at the maximum operating voltage on User Specification. Unless otherwise required, the power source shall be capable of delivering the current required to perform the test. Whenever required, current delivered to the device shall be determined based on initial resistance at room

temperature. This may be achieved by measuring the initial resistance at room temperature immediately preceding the test and calculating the necessary load resistance to deliver the current required by the specification.

2.3 Test conditions and Tolerances

2.3.1 Standard Stress Test Conditions: Unless otherwise specified herein, all stress tests shall be performed at the standard room condition. The standard room condition shall be defined as the temperature of 25 ± 5 °C with uncontrolled ambient air pressure and relative humidity. Whenever these conditions must be closely controlled in order to obtain reproducible results, for referee purposes, a temperature of 25 ± 3 °C, at uncontrolled ambient air pressure and relative humidity shall be used.

2.3.2 Standard Stress Test Tolerances: Unless otherwise specified, the tolerances for stress conditions shall be as follows:

Voltage:	± 2%	Weight:	± 2%
Current:	± 2%	Humidity:	± 5%
Temperature:	± 5°C	Length:	± 5%
Time:	+10% -0%		

2.3.3 Pre- and Post-Stress Test Conditions: Unless otherwise specified herein, all pre- and post-stress test evaluation measurements shall be performed at the minimum, room, and maximum rated temperatures. At the start of this test, the test chamber shall be controlled to test temperature ± 3 °C, at uncontrolled ambient air pressure and relative humidity. The temperature controller shall be capable of controlling the test chamber temperature to set temperature ± 2 °C.

3.0 TEST PROCEDURES

3.1 Physical requirement verification
Tests 9 and 10 of Table 14.

3.2 Electrical Performance Verification Test Procedures

3.2.1 Passive Resistance at Temperature: Devices shall be tested in accordance with AEC-Q200-004-001.

3.2.2 Time-to-Trip at Temperature: Devices shall be tested in accordance with AEC-Q200-004-002.

3.2.3 Hold Current at Temperature: Devices shall be tested in accordance with AEC-Q200-004-003 for hold current.

3.2.4 Sequence of Testing: Unless otherwise specified, the electrical performance verification tests shall be performed in the following order and state of the device:
Passive resistance at temperature: “As is” condition following any stress tests. For devices that require soldering for mounting on a test apparatus, devices shall be in room temperature and condition storage for at least 24 hours after-soldering prior to testing.
Time-to-trip at temperature: “As is” condition after passive resistance test.
Hold current at temperature: Test shall be performed after a minimum of 1 hour from the conclusion of a trip event such as time-to-trip test. The starting of hold current test shall not exceed three hours from the conclusion of the trip event.

3.2.5 Test Environment: Electrical performance verification tests shall be performed at the minimum, room, and maximum rated temperatures. The devices shall be tested, unless otherwise specified, in a non-forced air environment. The test chamber temperature shall be monitored

and controlled at a location that reasonably represents the general test chamber temperature and result in the ability to control the chamber temperature as required. Test samples shall be divided into three equal groups except when the samples are not equally divisible, the remaining one or two devices shall be included in the room temperature test group. The groups that are selected to be in a certain temperature group shall remain in the same temperature group for pre- and post-stress tests.

3.3 Environmental, Electrical, and Mechanical Stress Test Procedures

3.3.1 Operational Life: Parts shall be tested per MIL-STD-202 Method 108 with the following details:
Distance of temperature measurement from specimen: 10.16 cm minimum
Still-air Requirement: None - Circulation oven permitted provided that there is no direct impingement of air flow on devices under test.
Test Temperatures: At 85C (125C for 125 C parts)
Operating Conditions: Apply $I_{hold@T}$ in constant current mode with power on for 15 seconds and off for 15 seconds. Devices-under-test may be connected in series for simplification of the power delivery system.

3.3.2 Terminal Strength (Leaded only): Parts shall be tested per MIL-STD-202 Method 211 with the following details:

Test Condition A:

Applied Force: 2.27 Kg

Method of Holding the device: Device-under-test (DUT) shall be held using a strip of fiberglass loaded Teflon sheet that is bent around DUT in between the pant legs in a “U” shape. Two free ends of the strip shall be held in the jaw or vice. The load shall be applied to one lead at a time in the manner prescribed in MIL-STD-202 Method 211. The width of the strip shall be slightly less than the distance between the pant legs. The strip shall be secured to DUT by means of adhesive tape such as fiber-glass tape to prevent slippage.

Test Condition C:

Applied Force: 227 g

Post-stress visual examination: Prior to post-stress electrical tests examine the bend area for cracks or breakage of wire lead. with a microscope with magnification of no greater than 10.

3.3.3 Short Circuit Fault Current Durability:

Apply the maximum short circuit current (I_{SCMAX}) specified in the user specification through the device under test for 5 to 10 seconds. Then remove the current for a minimum of 2 minutes. Repeat for the number of cycles specified in the user specification, where $V_{POWER\ SUPPLY} = I_{SCMAX} X R_{TEST\ SYSTEM.}$ $V_{POWER\ SUPPLY,}$ however, shall not exceed rated voltage for the device, and to set I_{SCMAX}, a shorting buss bar shall be used across the DUT mounting clips.

The device shall be functional after the test as verified per post-stress tests that include visual inspection, resistance, time-to-trip verification, and hold current verification.

3.3.4 Fault Current Durability:

Apply a minimum of 6 times the rated hold current (I_{HOLD}) specified in the user specification through the device under test for 5 to 7 minutes and then remove for a minimum of 10 minutes. Repeat for the number of cycles specified in the user specification. The device shall be

functional after the test as verified per post-stress tests that include visual inspection, resistance, time-to-trip verification, and hold current verification.

3.3.5 End-of-life Mode Verification:

Use the devices that were subjected to the fault durability test. Apply enough current, long enough to trip the device (current shall be a minimum of 6 times I_{HOLD} specified in the user specification). Hold in the tripped condition for 5 to 10 seconds and then turn power off for a minimum of minute. Repeat for the number of cycles specified in the user specification.

After stressing, examine for burnt devices and measure resistance. The device shall exhibit PTC of resistance behavior or shall have a resistance value that is high enough to limit the current to the hold current (I_{HOLD}) specified for the device at the rated voltage specified in the user specification.

3.3.6 Jump Start Endurance:

Apply 26 volts across R_L in series with the device under test. Monitor the voltage across R_L with an oscilloscope or equivalent. Apply voltage for 1minute ± 3 seconds then turn off for a minimum of 2 minutes. Apply and remove voltage 3 times. $R_L \leq V_{max\ of\ device} / I_{hold}$. Resistance due to wire and other electrical connections and the source impedance of the power supply shall be included in the calculation of R_L

The device shall be functional after the test as verified per post-stress tests that include visual inspection, resistance, time-to-trip verification, and hold current verification.

3.3.7 Load Dump Endurance: Devices shall be tested in accordance with ISO7635-1 using Test Pulse number 5.

Apply ISO 7635-1 load dump voltage V_S across R_L and the device under test . Monitor the voltage across R_L with an oscilloscope or equivalent. The pulses shall be applied every 90 ± 30 seconds for a total of 10 pulses. $R_L \leq V_{max\ of\ device} / I_{hold}$. Resistance due to wire and other electrical connections and the source impedance of the power supply shall be included in the calculation of R_L

The device shall be functional after the test as verified per post-stress tests that include visual inspection, resistance, time-to-trip verification, and hold current verification.

Test Parameters:

V_s: The test pulse voltage shall be the rated device load dump voltage as defined in User Specification.
R_i: In accordance with the table below.
U_A: 13.5 ± 0.5 V
t_d: In accordance with the table below.
t_r: 5-10 ms

Vs (V)	Ri (□)	td (ms)
26.5	0.50	40
46.5	1.67	160
66.5	2.83	280
86.5	4.00	400

AEC-Q200-004-001

Resistance Measurement Method

1.0 SCOPE

1.1 **Purpose**: This AEC-Q200-004-001 covers methods used to measure resistance of PTC resettable devices while the devices are in the off state.

2.0 EQUIPMENT

2.1 **2-Wire Resistance Measurement Instrument**: A digital ohmmeter or multimeter measuring to at least 1% accuracy is required. The instrument shall be capable of making zero adjustment with the test clips shorted together to compensate for the lead resistance. An example of instruments capable of making 2 wire resistance measurements is Hewlett-Packard digital multimeter HP34401A, or equivalent.

2.2 **4-Wire Resistance Measurement Instrument**: A digital ohmmeter or multimeter measuring to at least 1% accuracy is required. The instrument shall be capable of applying the test current at the point of resistance measurement for accurately compensating for the test lead resistance. Examples of instruments capable of making 4 wire resistance measurements are Hewlett-Packard digital multimeter HP34401A, Valhalla Scientific 4150ATC Digital Ohmmeter, or equivalent.

3.0 PROCEDURE

Caution: The resistance of a resettable fuse is sensitive to temperature by nature. Instruments used to measure the resistance of PTC resettable devices must minimize heating of the test specimen. It is recommended that the device be handled using a pair of tweezers, or equivalent, to minimize influencing the resistance measurement due to the elevated temperature of fingers or hands. The devices shall be placed in the position in which the measurement is to take place and allow sufficient time for the device to reach the measurement temperature.

3.1 **Test Circuit, 2-Wire**: The measuring instrument may be connected to the test device with any suitable clip leads. This method shall be used to measure device resistance values of 20 ohms or higher.

3.2 **Test Circuit, 4-Wire**: The measuring instrument is generally connected to the test device with special Kelvin clip leads. If standard clip leads are used, the voltage leads must be the closer to the body of the device, and the current leads further from the body of the device. This method of resistance measurement shall be used to measure device resistance values of less than 20 ohms.

3.3 **Device Mounting and Resistance Measurement Location**: Resistance of devices shall be measured at the connection point to the fixture as defined in Paragraph 2.1.1 of AEC-Q200-004.

3.4 **Resistance Measurements for Devices Mounted with Heat**: Initial resistance of the devices that require heat for mounting onto test fixtures (e.g. soldering of SMD components) shall be the value measured at least 24 hours from the time of the heating operation.

AEC-Q200-004-002

Time-to-Trip Measurement Method

1.0 SCOPE

1.1 **Purpose**: The purpose of this test is to verify that a test specimen will trip within a specified length of time at a specified current.

2.0 EQUIPMENT

2.1 **Power Supply**: A power source capable of supplying the trip current specified in the user specification, at the voltage specified in the user specification. The source voltage must be controlled to ± 2%. The load resistor controls the source current.

2.2 **Load Resistor**: A load resistor to adjust the current through the test specimen to ± 2% of the trip current specified in the user specification, when the power source is set for the maximum operating voltage specified in the user specification.

2.3 **Parametric Measurement Instruments**: A system for measuring either the voltage across the test specimen, or the current through it (or both), as a function of time. The time resolution of the system needs to be 100 milliseconds or better, unless otherwise specified in the user specification. The voltage or current needs to be determined to be an accuracy of ± 2%. Digital equipment is suggested, for ease in storing and transferring information. Suitable systems include digital oscilloscopes, A/D converters, and computer-controlled multimeters.

3.0 PROCEDURES

3.1 **Device Mounting**: Test samples shall be mounted in accordance with Paragraph 2.1.1 of AEC-Q200-004. The devices shall be tested individually or multiple devices in parallel. When multiple devices are connected in parallel, the current through each device shall be controlled and monitored separately. In addition, time-to-trip measurement shall be measured individually

3.2 **Resistance**: Resistance of test samples shall be measured prior to the time-to-trip test and one hour after the conclusion of the test in accordance with AEC-Q200-004-001.

3.3 **Non-Forced Air Ambient**: The time-to-trip of PTC resettable devices may be influenced substantially by air flow. As such, there shall be no air circulation around the test specimen during the test, including air flow due to body motion. Naturally convective airflow due to heating and cooling of the test specimen shall be allowed.

3.4 **Test Temperature**: The devices shall be tested at the temperature specified in this specification or User Specification. The test specimens shall be allowed to equilibrate at the specified temperature for a minimum of 5 minutes.

3.5 **Test Current**: The time-to-trip evaluation test current level shall be as specified in User Specification. In cases where the test current is not specified, 5 times the $I_{hold@T}$ shall be used.

3.6. **Test Sequence:** The time-to-trip test shall be performed after a resistance measurement. The device shall not experience any trip event(s) after manufacturing, soldering, or stress testing, whichever is the most recent event, prior to the time-to-trip test.

AEC-Q200-004-003

Hold Current Measurement Method

1.0 SCOPE

1.1 **Purpose**: The purpose of this test is to verify that a test specimen will pass a specified current without tripping.

2.0 EQUIPMENT

2.1 **Power Supply**: A power source capable of supplying the trip current specified in the user specification, at the voltage specified in the user specification. The source voltage must be controlled to ± 2%. The load resistor controls the source current.

2.2 **Load Resistor**: A load resistor to adjust the current through the test specimen to ± 1% of the trip current specified in the user specification, when the power source is set for the maximum operating voltage specified in the user specification.

2.3 **Parametric Measurement Instruments**: A system for measuring either the voltage across the test specimen, or the current through it (or both), as a function of time. The voltage or current needs to be determined to an accuracy of ± 1%. Digital equipment is suggested, for ease in storing and transferring information. Suitable systems include digital oscilloscopes, A/D converters, and computer-controlled multimeters.

2.4 **Elapsed Time Measurement Device**: Commonly used time measuring instrument capable of timing the hold current test duration, e.g. stop watch.

3.0 PROCEDURES

3.1 **Device Mounting**: Test samples shall be mounted in accordance with Paragraph 2.1.1 of AEC-Q200-004. The devices may be tested individually or in groups. If tested in a group, the devices shall be connected in series.

3.2 **Resistance**: Resistance of test samples shall be measured prior to the hold current test and one hour after the conclusion of the test in accordance with AEC-Q200-004-001.

3.3 **Non-Forced Air Ambient:** The hold current capability of PTC resettable devices may be influenced substantially by airflow. As such, there shall be no air circulation around the test specimen during the test, including airflow due to body motion. Naturally convective airflow due to heating and cooling of the test specimen shall be allowed.

3.4 **Test Temperature**: The devices shall be tested at the temperature specified in this specification or User Specification. The test specimens shall be allowed to equilibrate at the specified temperature for a minimum of 5 minutes.

3.5 **Test Current**: The hold current level shall be as specified in User Specification as $I_{hold@T}$.

3.6 **Test Sequence**: The hold current evaluation test shall be performed at least one hour, but not more than three hours, after the most recent trip event. In most cases, this trip event will be a time-to-trip evaluation test.

3.7 **Test duration**: The hold current as defined in accordance with User Specification shall be applied to the test specimen for 15 minutes or more.

3.8 **Pass/Fail Criteria**: The samples that pass the hold current evaluation test shall be capable of conducting specified $I_{hold@T}$ for a minimum of 15 minutes.

AEC-Q200-004-004

Trip Current Measurement Method

1.0 SCOPE

1.1 **Purpose**: The purpose of this test is to verify that a test specimen will trip at a specified current.

2.0 EQUIPMENT

2.1 **Power Supply**: A power source capable of supplying the trip current specified in the user specification, at the voltage specified in the user specification. The source voltage must be controlled to ± 2%.

2.2 **Load Resistor**: A load resistor to adjust the current through the test specimen to ± 2% of the trip current specified in the user specification, when the power source is set for the maximum operating voltage specified in the user specification.

2.3 **Parametric Measurement Instruments**: A system for measuring either the voltage across the test specimen, or the current through it (or both). The voltage or current needs to be determined to an accuracy of ± 2%. Digital equipment is suggested, for ease in storing and transferring information. Suitable systems include digital oscilloscopes, A/D converters, and computer-controlled multimeters.

2.4 **Elapsed Time Measurement Device**: Simple time measuring instrument capable of timing the trip current test duration.

3.0 PROCEDURES

3.1 **Device Mounting**: Test samples shall be mounted in accordance with Paragraph 2.1.1 of AEC-Q200-004 The devices shall be tested individually or connected to the power supply in parallel.

3.2 **Resistance**: Resistance of test samples shall be measured prior to the trip current test and one hour after the conclusion of the test in accordance with AEC-Q200-004-001.

3.3 **Non-Forced Air Ambient**: The trip current capability of PTC resettable devices may be influenced substantially by airflow. As such, there shall be no air circulation around the test specimen during the test, including airflow due to body motion. Naturally convective airflow due to heating and cooling of the test specimen shall be allowed.

3.4 **Test Temperature**: The devices shall be tested at the temperature specified in this specification or User Specification. The test specimens shall be allowed to equilibrate at the specified temperature for minimum of 5 minutes.

3.5 **Test Current**: The trip current level shall be as specified in User Specification as $I_{trip@T}$.

3.6 **Test Sequence**: The trip current evaluation test shall be performed on devices that have not been tripped. If a heating process, such as soldering, is necessary to perform tests on a test fixture, the device shall be conditioned at the standard room condition for at least 24 hours prior to the testing of the trip current.

3.7 **Test duration**: The trip current as defined in accordance with User Specification shall be applied to the test specimen for 15 minutes or until the device trips, whichever occurs first.

3.8 **Pass/Fail Criteria:** The samples that pass the trip current evaluation test shall trip at the specified $\mathbf{I_{trip@T}}$ in 15 minutes or less.

AEC-Q200-004-005

Power Dissipation Measurement Method

1.0 SCOPE

1.1 **Description**: The purpose of this test is to determine the amount of power dissipated by a device in a standard environment after it has stabilized in the tripped state.

2.0 EQUIPMENT

2.1 **Power Supply**: A power source capable of supplying the trip current specified in the user specification, at the voltage specified in the user specification. The source may be either ac or dc, unless the type is specified in the user specification. The source voltage must be controlled to ± 2%. The load resistor controls the source current.

2.2 **Load Resistor**: A load resistor to adjust the current through the test specimen to ± 2% of the trip current specified in the user specification, when the power source is set for the maximum operating voltage specified in the user specification.

2.3 **Parametric Measurement Instruments**: A system for measuring either the voltage across the test specimen and the current through the device-under-test. The voltage or current needs to be determined to an accuracy of ± 2%. Digital equipment is suggested, for ease in storing and transferring information. Suitable systems include digital oscilloscopes, A/D converters, and computer-controlled multimeters, or equivalent.

3.0 PROCEDURE

3.1 **Device Mounting**: Test samples shall be mounted in accordance with Paragraph 2.1.1 of AEC-Q200-004. The devices may be connected to the power source in parallel.

3.2 **Resistance**: Resistance of test samples shall be measured prior to the power dissipation test and one hour after the conclusion of the test in accordance with AEC-Q200-004-001.

3.3 **Non-Forced Air Ambient**: The power dissipation of PTC resettable devices may be influenced substantially by airflow. As such, there shall be no air circulation around the test specimen during the test, including airflow due to body motion. Naturally convective airflow due to heating and cooling of the test specimen shall be allowed.

3.4 Test Temperature

The devices shall be tested at the temperature specified in this specification or User Specification. The test specimens shall be allowed to equilibrate at the specified temperature for minimum of 5 minutes.

3.5 Test Current:

The minimum power dissipation test current level shall be the trip current as specified in User Specification as $I_{trip@T}$.

3.6 Test Sequence

The power dissipation measurement shall be performed on devices that are in the tripped state. Once the test sample reaches the tripped state, measure the voltage across the device and the current through the device. The power dissipation may be calculated from the voltage and current measurements

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
	March 15, 2000	Initial Release.

Attachment 5

PASSIVE COMPONENT
SURFACE MOUNTED DEVICES

Board Flex / Terminal Bond Strength Test

METHOD - 005

PASSIVE COMPONENT
Board Flex / Terminal Bond Strength Test

1.0 SCOPE

1.1 DESCRIPTION:

This specification establishes the procedure and criteria for evaluating the Terminal Strength of a Surface Mount Component when mounted on a PCB during a Board Flex.

1.2 Reference Documents:

Not Applicable

2.0 EQUIPMENT:

2.1 Test Apparatus:

The apparatus required for testing shall be equivalent to the fixture shown in Figure 1.

3.0 TEST PROCEDURE:

3.1 Sample Size:

The total number of components and lots to be tested are listed in Table 1 of AEC-Q200 specification.

3.2 Test Environment :

1. Part mounted on an FR4 board provided by the Supplier for the part being tested with the following requirements:

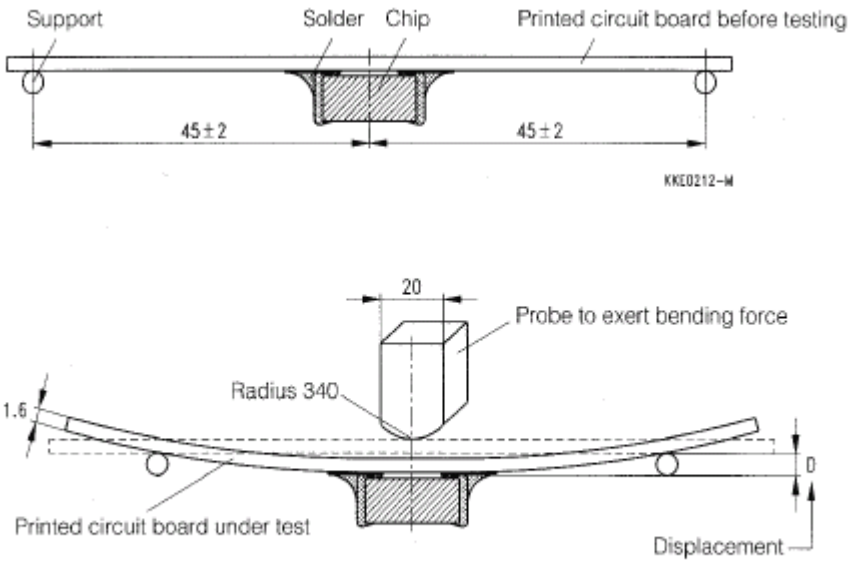
2. Land pattern is supplier's standard for part being tested.

3. Part mounted on a 100mm X 40mm FR4 PCB board, which is 1.6mm ± 0.2 mm thick and has a Layer-thickness 35 µm ± 10 µm. Part should be mounted using the following Soldering Reflow profile:

   Preheat temperature (125°C ± 25°C) max 120 sec.
   Time above 183°C 60 sec. – 150 sec.
   Max. ramp up (183°C to peak) ≤ 3°C / sec.
   Peak temperature 235°C + 5°C
   Time in peak temperature 10 sec. – 20 sec.
   Ramp down rate ≤ 6°C / sec.

4. Place the 100mm X 40mm board into a fixture similar to the one shown in Figure 1 with the component facing down. The apparatus shall consist of mechanical means to apply a force which will bend the board (D) x = 2 mm minimum (or as defined in the customer specification or Q200). The duration of the applied forces shall be 60 (+ 5) Sec. The force is to be applied only once to the board.

Figure 1 Test Fixture



3.3 Measurement:

Prior to beam load testing, complete the external Visual test in Q200. A test monitor shall be used to detect when a part cracks or a termination failure occurs. (example: Megohmeter attached with leads during the time the force is being applied to a Ceramic Capacitor. A crack would cause a deflection of the needle towards zero.)

3.4 Failure:

A failure is when a part cracks or causes a change in the parametric being monitored.

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Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
	February 10, 2005	Initial Release.

Attachment 6

AEC - Q200 - 006

Terminal Strength (SMD) / Shear Stress Test

METHOD - 006

PASSIVE COMPONENT
Terminal Strength (SMD) / Shear Stress Test

1.0 SCOPE:

The purpose of this test is to verify that the component terminations can withstand axial stresses that are likely to be applied during normal manufacturing and handling of a finished printed circuit board (PCB) assembly.

1.1 DESCRIPTION:

This test is designed to evaluate the strength of the solder bond between terminations/leads of a surface mounted device and a specified copper pattern on glass epoxy circuit board.

1.2 Reference Documents:

None.

2.0 EQUIPMENT:

Unless otherwise specified, the SMD shall be tested while mounted onto a .062 inch thick FR-4 PCB using 1 ounce of Copper. The Supplier shall use the preferred pad layout for the device being tested. The Supplier shall provide parts placed and reflowed on the test coupon and provided as part of the qualification package. (See Figure 1 below)

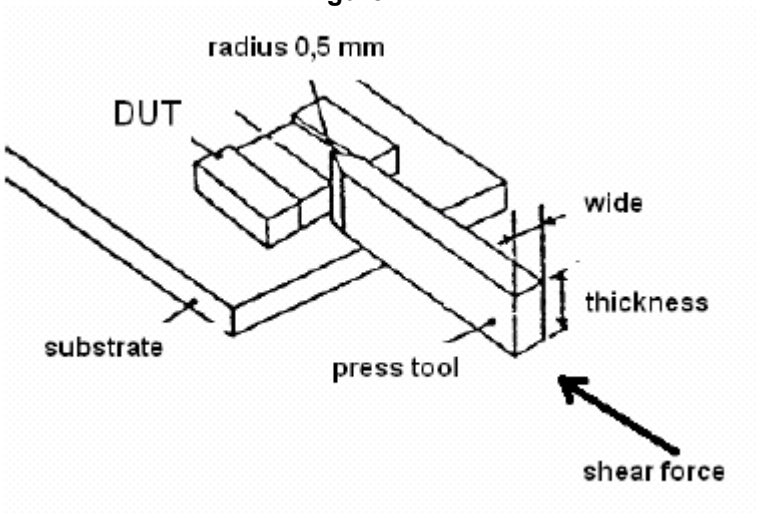
2.1 Test Apparatus:

See Figure 1

3.0 TEST PROCEDURE:

With the component mounted on a PCB obtained from the Supplier with the device to be tested, apply a 17.7 N (1.8 Kg) force to the side of a device being tested. This force shall be applied for 60 +1 seconds. Also the force shall be applied gradually as not to apply a shock to the component being tested. (See Figure 1)

Figure 1



Magnification of 20X or greater may be employed for inspection of the mechanical integrity of the device body, terminals and body/terminal junction. Before, during and after the test, the device shall comply with all electrical requirements stated in this specification.

3.1 Sample Size:

The total number of components and lots to be tested is listed in Table 1 of AEC-Q200 specification.

3.2 Pre and post-measurement:

Visual and Electrical characterization of devices are to be performed at room temperature per device specification.

4.0 FAILURE CRITERIA

The failure criteria are governed by not meeting the device specification, along with evidence of cracking or part being sheared off from its pad.

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
	February 15, 2005	Initial Release.

Attachment 7

AEC - Q200 - 007

VOLTAGE SURGE TEST

METHOD - 007

PASSIVE COMPONENT VOLTAGE SURGE TEST

1.0 SCOPE:

Aluminum Electrolytic Capacitors

1.1 DESCRIPTION:

The purpose of this specification is to assure a device will withstand voltage surges at the surge voltage rating of the device's specification.

1.2 Reference Documents:

Not Applicable

2.0 EQUIPMENT:

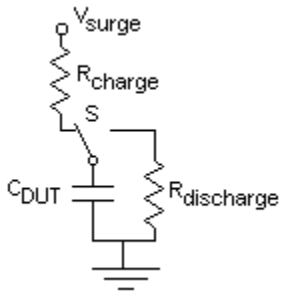
2.1 Test Apparatus:

The following items are required when performing this test:

a) A circuit board with test circuit shown in Figure 1.

b) A regulated, variable voltage power supply capable of maintaining DC voltage at the surge voltage, V_{surge}, a current level greater than limit created by the charging resistor, R_{charge} (current limit > V_{surge}/R_{charge}).

Figure 1. Test Circuit.



3.0 TEST PROCEDURE:

3.1 Sample Size:

The total number of components and lots to be tested are listed in Table 1 of AEC-Q200 specification.

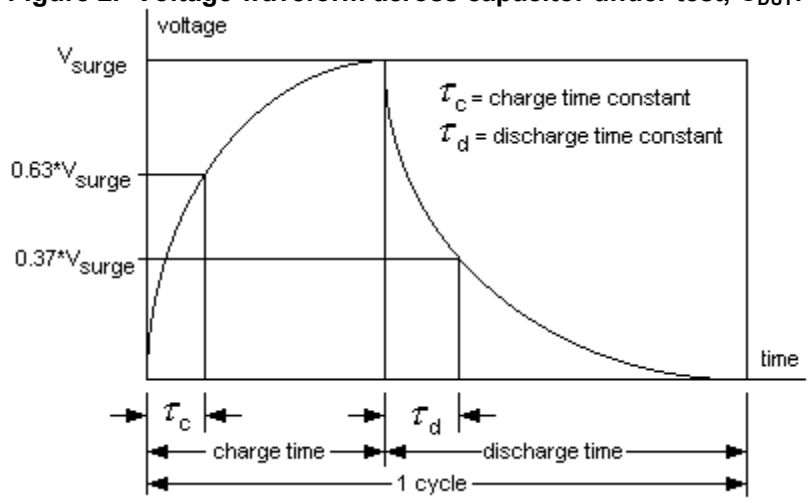
3.2 Pre and post-measurement:

Electrical characterization of devices at room temperature per device specification.

3.3 Surge test:

Subject capacitor under test, C_{DUT}, to the voltage waveform in Figure 2. The charge and discharge time constants, ratio of surge voltage to rated voltage, number of test cycles, duration of charging and discharge periods, time between cycles, and temperature (if different than 25+/-5C) shall be specified in the device specification.

Figure 2. Voltage waveform across capacitor under test, C_{DUT}.



4.0 FAILURE CRITERIA

Failure criteria is governed by the device specification.

Automotive Electronics Council
Component Technical Committee

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
	February 8, 2005	Initial Release

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